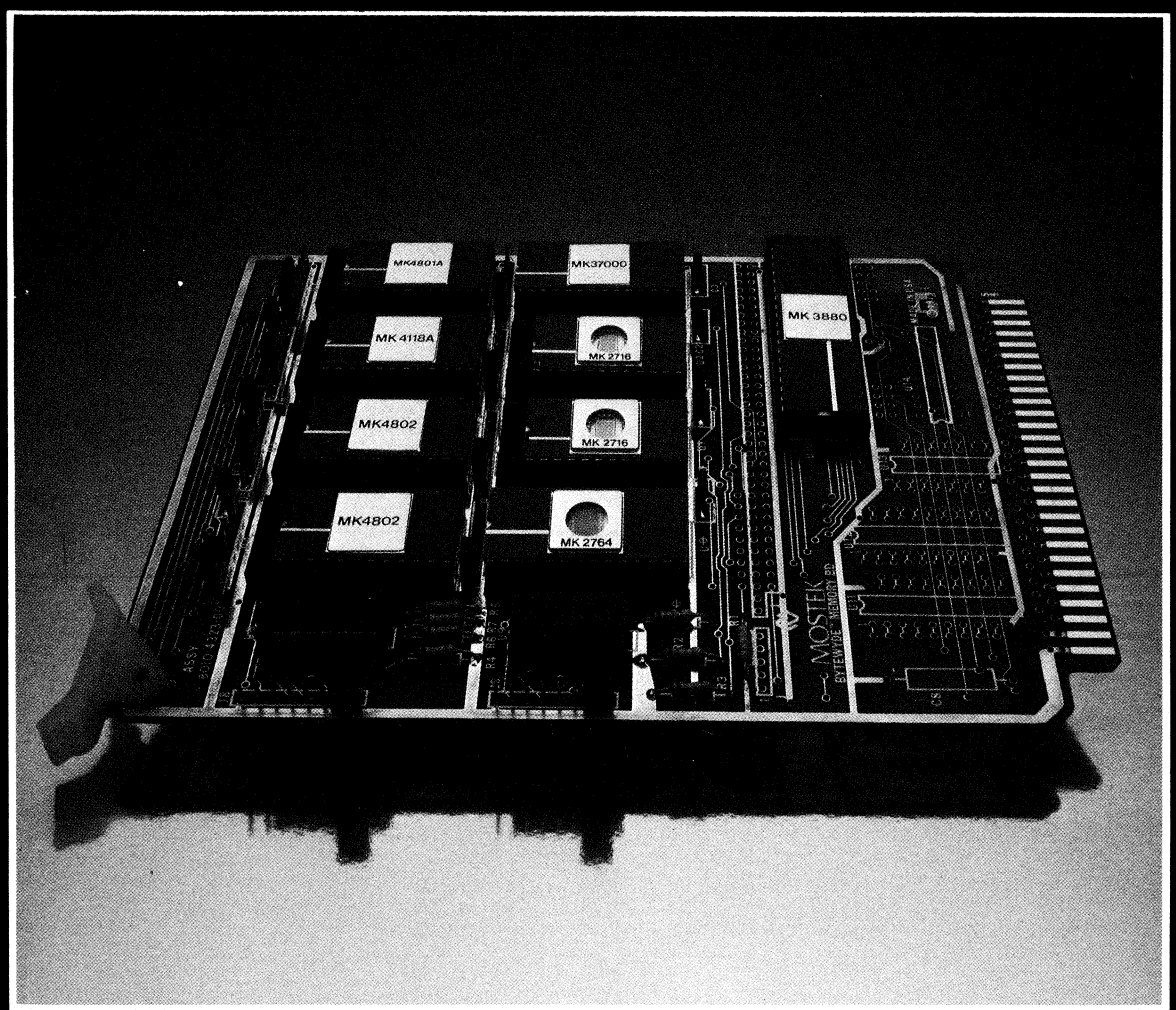
MOSTEK 1981

BYTEWYDE MEMORY DATA BOOK



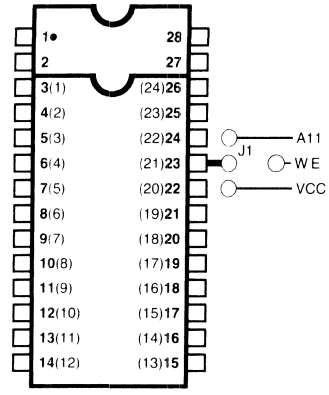
1981
BYTEWYDE Products
Data Book

PRINTED IN USA October 1980
STD No. 14819

MOSTEK'S BYTEWYDE STATIC MEMORY FAMILY

Memory Type	Part Number	Capacity	Package	Jumper J1
ROM	MK34000	2K × 8	24 Pin	NC
ROM	MK37000	8K × 8	28 Pin	A11
ROM		32K × 8 △	28 Pin	A11
RAM	MK4802	2K × 8	24 Pin	WE
RAM		4K × 8 △	28 Pin	A11
RAM	MK4118A/4801A	1K × 8	24 Pin	WE
EPROM	MK2716	2K × 8	24 Pin	VCC
EPROM	MK2764 △	8K × 8	28 Pin	A11

△ available 1981



4118/A 4801A	4802	34000	2716	4K × 8	37000	32K × 8	2764		2764	32K × 8	37000	4K × 8	2716	34000	4802	4118A 4801A
				NC	NC	A14	NC	1 28	VCC	VCC	VCC	VCC				
				NC	A12	A12	A12	2 27	NC	NC	NC	$\overline{WE}$				
A7	A7	A7	A7	A7	A7	A7	A7	3(1) (24)26	NC	A13	NC	NC	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6	A6	4(2) (23)25	A8	A8	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	A5	A5	5(3) (22)24	A9	A9	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	A4	A4	6(4) (21)23	A11	A11	A11	A11	VPP	NC	$\overline{WE}$	$\overline{WE}$
A3	A3	A3	A3	A3	A3	A3	A3	7(5) (20)22	$\overline{OE}$ VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2	A2	A2	A2	8(6) (19)21	A10	A/$\overline{O}$	A10	A/$\overline{O}$	A10	A10	A10	NC
A1	A1	A1	A1	A1	A1	A1	A1	9(7) (18)20	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0	A0	A0	A0	10(8) (17)19	D7	D7	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	D0	D0	D0	11(9) (16)18	D6	D6	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	D1	D1	D1	12(10) (15)17	D5	D5	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	D2	D2	D2	13(11) (14)16	D4	D4	D4	D4	D4	D4	D4	D4
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	14(12) (13)15	D3	D3	D3	D3	D3	D3	D3	D3

Parenthesis Indicates Pin Number of 24 Pin Packages.
24 Pin Devices are Lower Justified in Pins 3 Thru 26 of 28 Pin Socket

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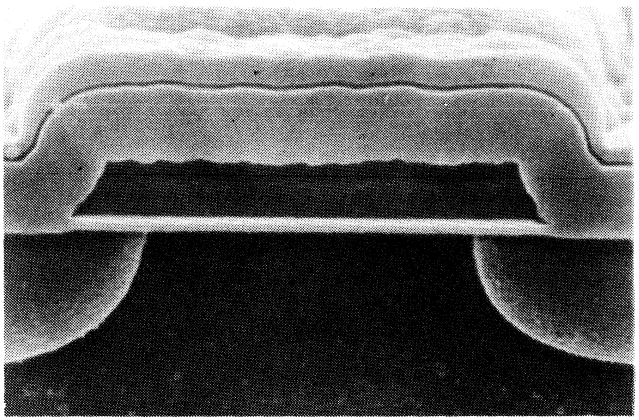
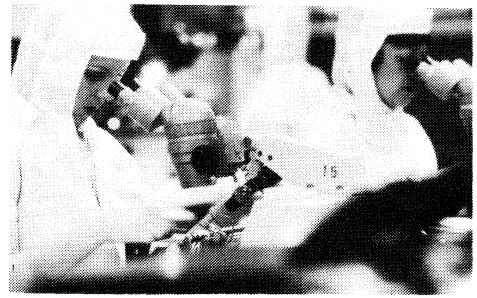
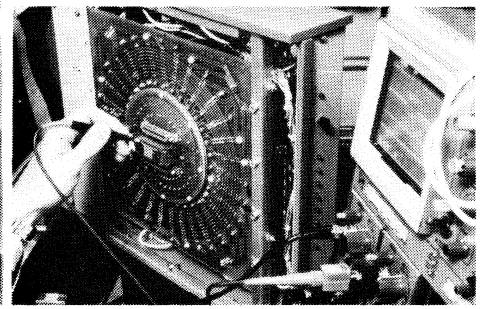






TECHNOLOGY

From the beginning, Mostek has been recognized as an innovator. In 1970, Mostek developed the MK4006 1K dynamic RAM and the world's first single-chip calculator circuit, the MK6010. These technical breakthroughs proved the benefits of ion-implantation and cost-effectiveness of MOS. Now, Mostek represents one of the industry's most productive bases of MOS/LSI technology. Each innovation - in memories, microcomputers and telecommunications - adds to that technological capability.

QUALITY

The worth of a Mostek product is measured by its quality. How well it's designed, manufactured and tested. How well it works in your system.

In design, production and testing, our goal is meeting the spec every time. This goal requires a strict discipline, both from the company and from the individual. This discipline, coupled with a very personal pride, has driven Mostek to build in quality at every level, until every product we take to the market is as well-engineered as can be found in the industry.

PRODUCTION CAPABILITY

Mostek's commitment to increasing production capability has made us the world's largest manufacturer of dynamic RAMs. In 1979 we shipped 25 million 4K and 16K dynamic RAMs. We built our first telecommunication tone dialer in 1974; since then, we've shipped over 5 million telecom circuits. The MK3870 single-chip microprocessor is also a large volume product with over two million in application around the world. To meet the demand for our products, production capability must be constantly increased. To accomplish this, Mostek has been in a constant process of expanding and refining our production capabilities.

THE PRODUCTS

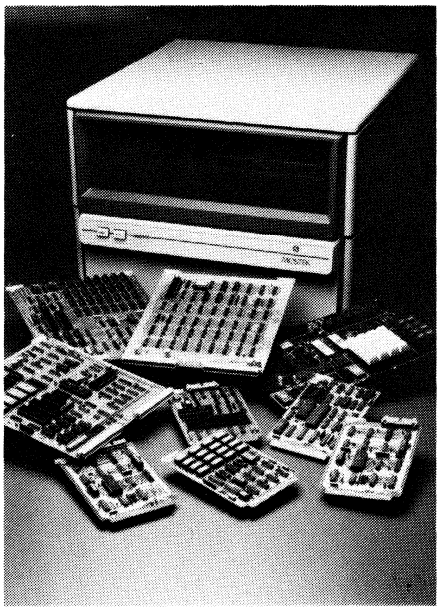
Telecommunications and Industrial Products

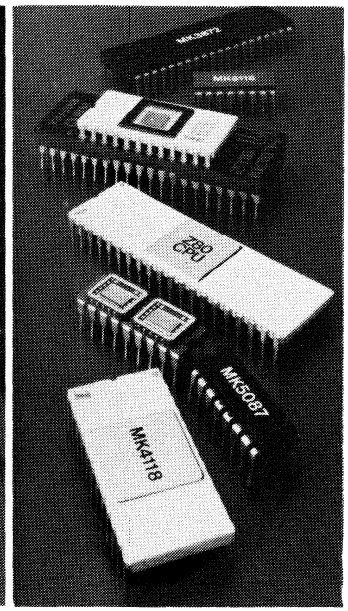
Mostek has made a solid commitment to telecommunications with a new generation of products, such as Integrated Pulse Dialers, Tone Dialers, CODECs, monolithic filters, tone receivers, A/D converters and counter time-base circuits.

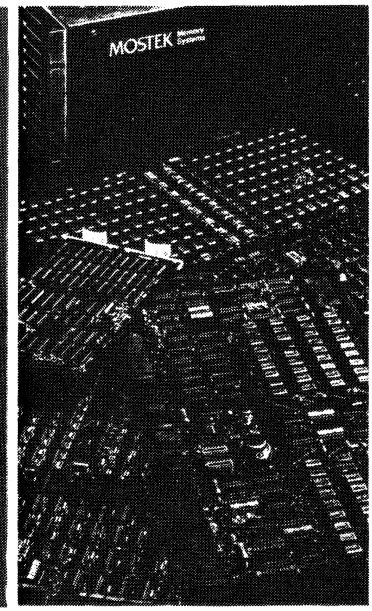
Since 1974 over five million telecom circuits have been shipped, making Mostek the leading supplier of tone/pulse dialers and CODECs.

Memory Products

Through innovations in both circuit







design, wafer processing and production, Mostek has become the industry's leading supplier of memory products.

An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory families.

Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is the highest performance 8-bit microcomputer available today. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM, and I/O, all in the same socket. The MK3874 EPROM version supports and prototypes the entire family.

Microcomputer Systems

Supporting the entire component product line is the powerful MATRIX™ microcomputer development system, a Z80-based, dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC, FORTRAN, and PASCAL are also available for use on the MATRIX.

Mostek's MD Series™ features both stand-alone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

The STD-Z80 BUS is a multi-sourced motherboard interconnect system designed to handle any MDX card in any card slot.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC and Data General minicomputers.

Mostek also offers special purpose and custom memory boards for special applications.

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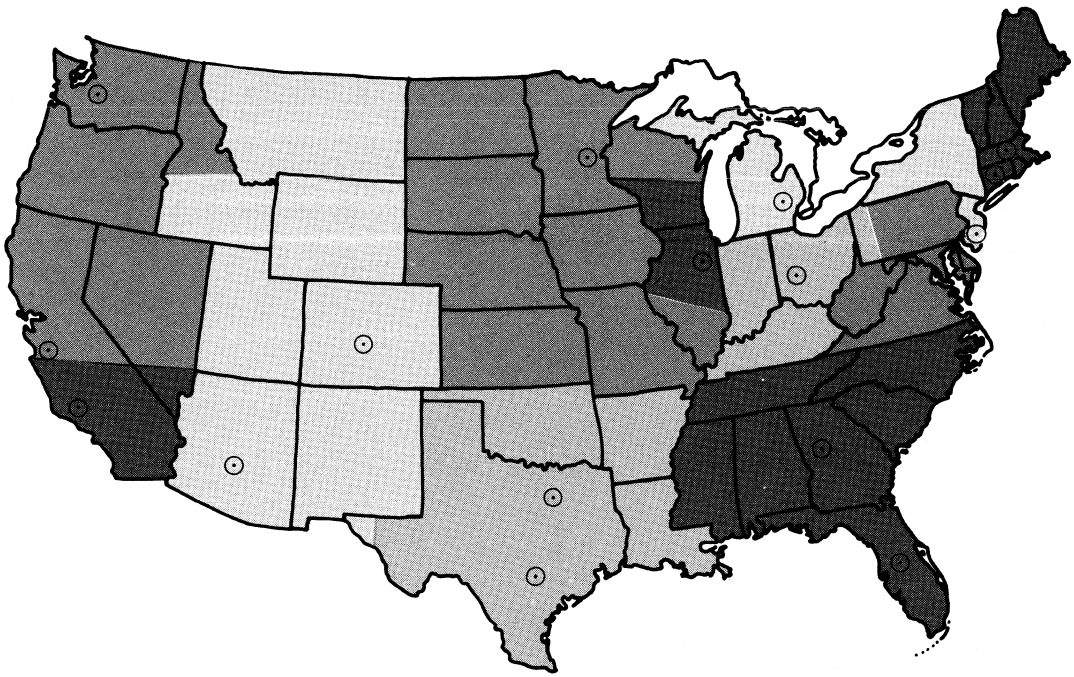

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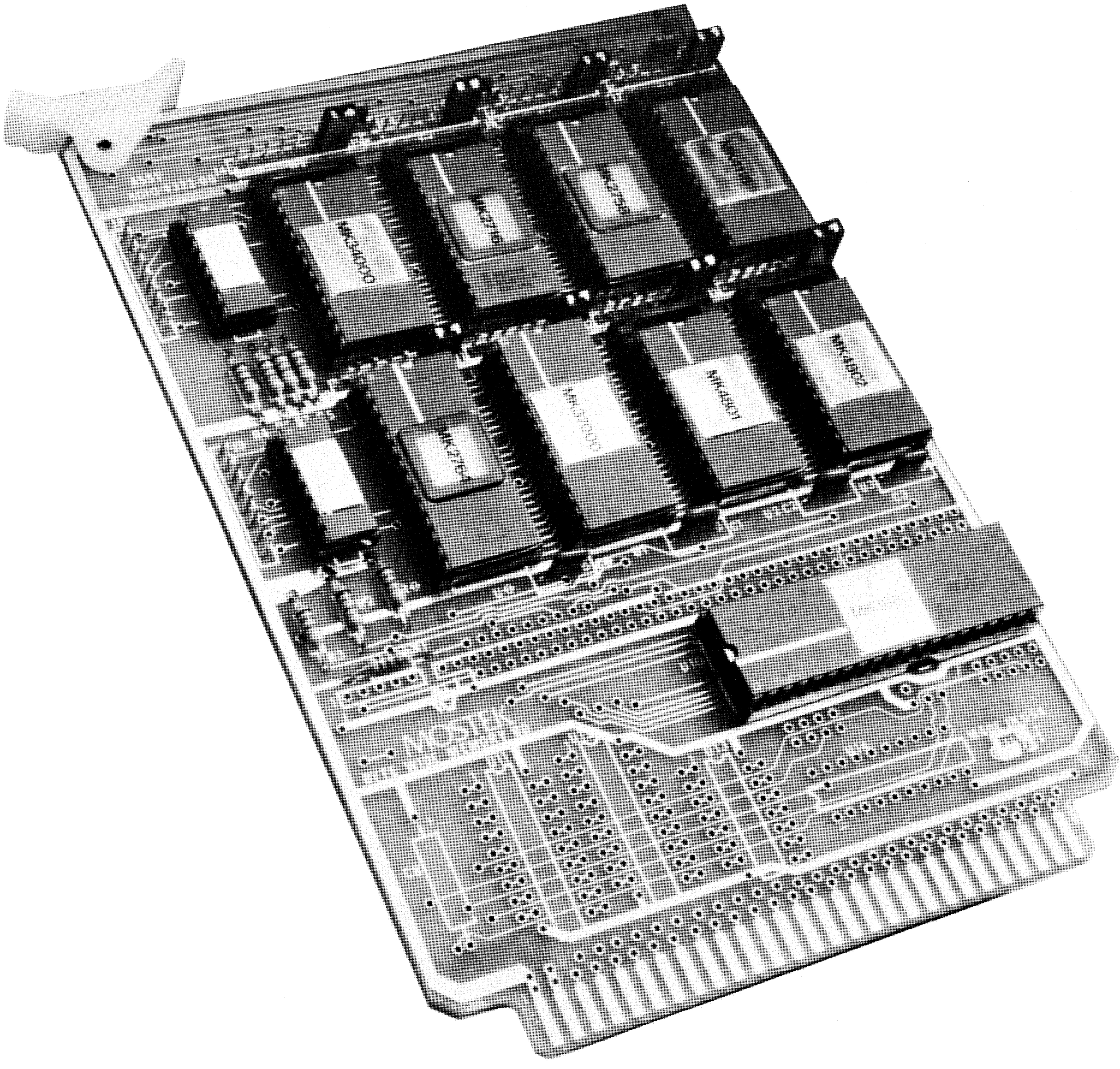
MOSTEK®

BYTEWYDE STATIC MEMORY FAMILY

Application Note

DESIGNING MICROPROCESSOR MEMORY WITH MOSTEK'S BYTEWYDE CONCEPT


MK34000
MK2716
MK2758
MK2764
MK37000
MK4801
MK4802
MOSTEK

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LIST OF TABLES AND FIGURES

INTRODUCTION

The term "byte wide" refers to a memory element which stores an 8-bit data word (byte) for each address location. Since all microprocessors are byte oriented, byte wide memories are a natural building block for microprocessors.

Mostek's BYTEWYDE concept ushers in a new era of compatibility for memory designs. For the first time RAM, ROM, and EPROM can be interchanged in the same socket because they share a common pin out. (Figure 1) Upgradeability is assured by carefully planned next generation devices. This flexibility allows for the design of an obsolescent proof memory system.

The members of Mostek's BYTEWYDE family feature **chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls to facilitate simple interface to microprocessors and** enhance performance. The BYTEWYDE memories can meet the requirements of even the fastest microprocessors.

Standard 24 and 28 pin dual-in-line packages were chosen to implement the BYTEWYDE family. To obtain maximum flexibility, a 28 pin socket site can be used to accept both the 24 and 28 pin devices. (Figure 2) The same BYTEWYDE memory design can remain cost effective and density competitive by upgrading to future components of the family. This prolonged product life increases return on the engineering investment and economies to scale. Mostek is committed to pin compatibility between today's memories and future generation devices. (Figure 3)

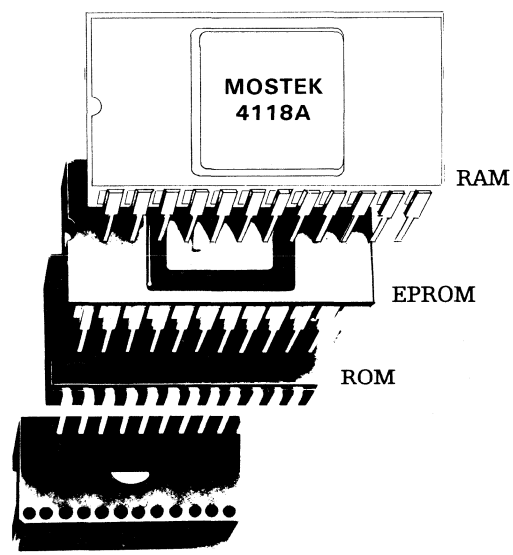
Interchangeability between RAM, ROM and EPROM is a key issue in Mostek's BYTEWYDE approach. The distinction between these devices is primarily data retention, when viewed from the system level. Therefore, design constraints are removed since early definition of the quantity of RAM versus ROM (EPROM) is not needed. End products are, as a result, more adaptive to changing market needs by substitution of the different memory devices.

Microprocessor memories using an organization of N words x 8 bits (byte) are an optimum building block. With a trend towards distributed processor architecture, BYTEWYDE memories will have an even more pronounced effect on implementation. In distributed systems the overall memory required can be large, but the concentration of memory in any one computing element is comparatively small. A typical requirement for a computing element might be 12K bytes. Using BYTEWYDE memories, between 2 and 8 devices would be needed, depending upon the mix of RAM/ROM EPROM.

Substituting the necessary number of 16K or 64K one bit wide memories in this application will quickly show the advantage of the BYTEWYDE approach. (Figure 4)

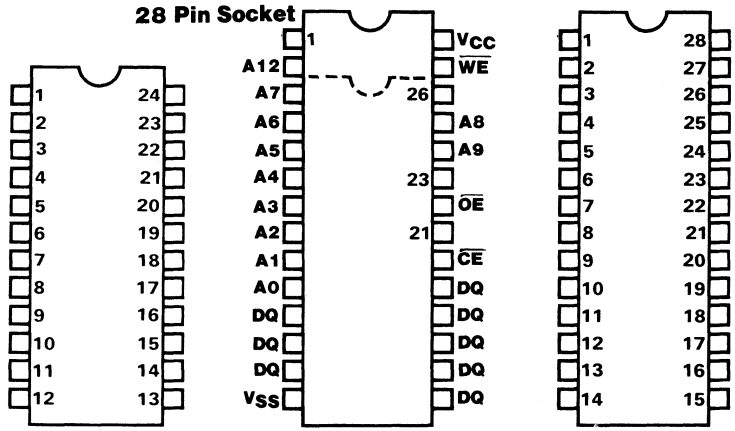
Mostek's BYTEWYDE memories are easy to use. Adequate control functions are provided to minimize interface complexity and enhance performance. The static characteristics of these memories eliminate the need for refresh circuitry. The simplicity of interfacing microprocessors to a Mostek BYTEWYDE memory array has been reduced to merely connecting address, data lines, and control signals. (Figure 5)

BYTEWYDE FAMILY CONCEPT
INTERCHANGEABILITY
Figure 1



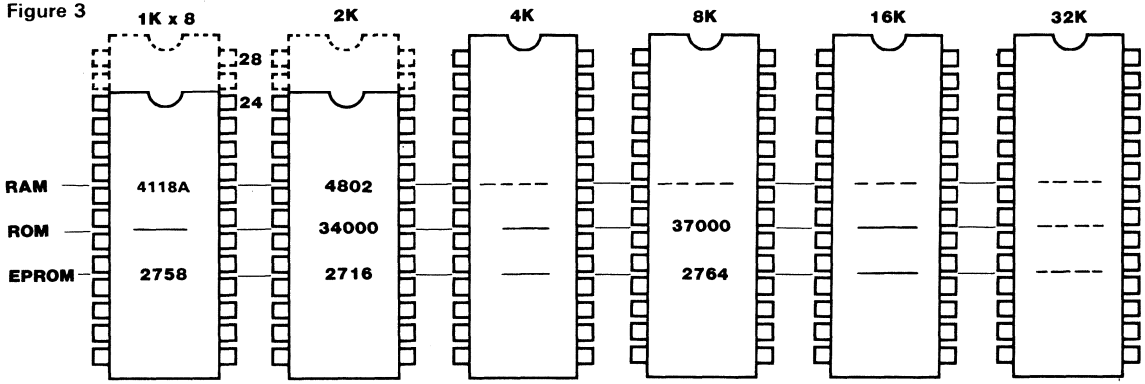
BYTEWYDE FAMILY CONCEPT - PIN COMPATIBILITY

Figure 2



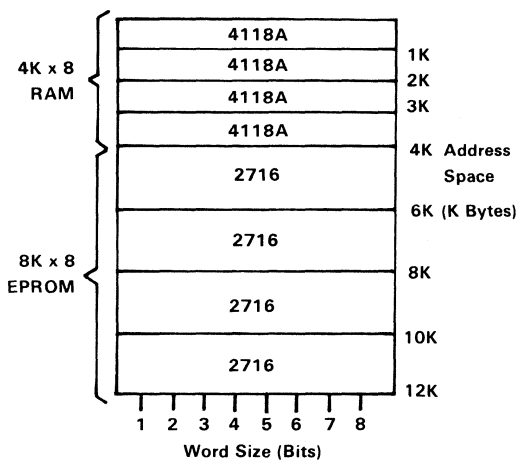
BYTEWYDE FAMILY CONCEPT - DENSITY UPGRADE

Figure 3



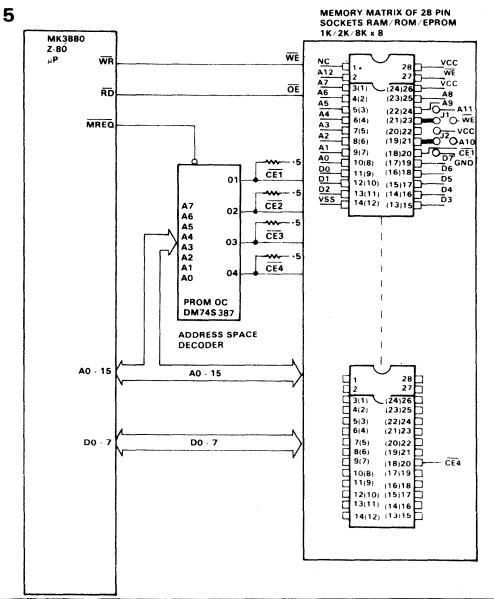
BYTEWYDE FAMILY CONCEPT - ORGANIZATION

Figure 4



BYTEWYDE FAMILY CONCEPT - EASY INTERFACE

Figure 5



BYTEWYDE CONTROL FUNCTIONS

A common difficulty experienced when interfacing memory on a shared data bus as found in a microprocessor system is bus contention. Bus contention is a term used to describe the condition in which two or more output buffers on the same bus line are enabled. These output buffers may reside in different memory devices within an array, peripheral interfaces, microprocessors, or any of the above. If suitable control functions are provided on each memory, data bus timing becomes well defined and the problem goes away without performance degradation.

A BYTEWYDE memory provides two control functions so that system performance will not be compromised for lack of output buffer control. Memory busses are commonly constructed with three levels of complexity. In the simplest case the bus has unidirectional data flow. A more complex bidirectional data bus allows data to flow into and out of the memory on the same lines but at different times thus conserving package pins, printed circuit board track, and connectors. To further conserve lines, addresses are sometimes multiplexed with a bidirectional data bus. In any of these cases the system designer must be able to guarantee that for any point in time the bus be defined for data in, data out, or address. In this way bus contention is eliminated.

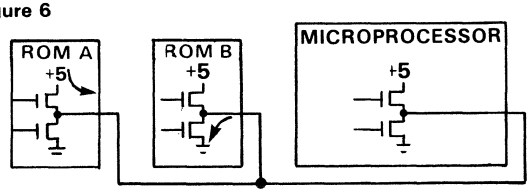
Bus contention is defined to be a condition when two or more output buffers on the same line are simultaneously turned on.
In Figure 6 ROM A and ROM B are said to be in bus contention because A is sourcing current "1" and B is sinking current "0" at the same point in time creating a short circuit across the power supply. For proper system operation ROM A must go to a high impedance state prior to ROM B output turning on. This break before make characteristic is essential for all multi output bus schemes. Short periods of bus contention normally cause no catastrophic damage but do generate large amounts of system noise. This noise can cause an obscure system malfunction which does not lend to straight forward troubleshooting procedures. For reliable system operation bus contention must be avoided. The timing diagram Figure 6 shows ROMA and ROM B implemented with output buffers controlled solely by $\overline{CE}$ (chip enable).

In this case the output buffer enable time must be longer than the disable time when switching from A to B to insure a contention free bus; however, this is difficult to achieve in practice because of unit to unit variations among devices. The second data bus waveform shows the contention problem when $\overline{CE}$ enable B time is less than $\overline{CE}$ disable A time.

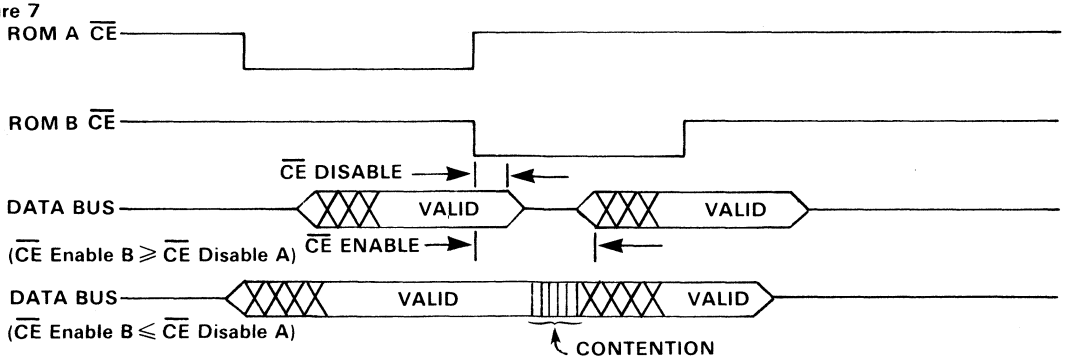
If a fast $\overline{OE}$ (output enable) control is provided in addition to the $\overline{CE}$ control no constraints are placed on $\overline{CE}$ for bus contention. In this way $\overline{CE}$ is reserved for device selection and $\overline{OE}$ for buffer control. When a device is given a $\overline{CE}$ it is singled out in a matrix as the device to go into cycle. The selected device then powers up for the cycle. After the device is selected, at a time when bus contention is not a problem, $\overline{OE}$ can be used to gate data on and off the bus. This freedom to control the bus with the $\overline{OE}$ allows the next cycle to be initiated with $\overline{CE}$ prior to the bus being released from the previous cycle thus enhancing performance or widening operating margin.

When a bidirectional data bus scheme is configured the possibility of another form of bus contention exists when a write is followed by a read. Typically the data in for a write must be held valid until the completion of the write cycle. During this write time data is flowing into the memory and is being driven by the output of the microprocessor. If a read cycle immediately follows a write cycle the data bus has to switch from data in to data out. If the read device output is solely controlled by

OUTPUT BUFFER CONFIGURATIONS (SHARED DATA BUS)
Figure 6



READ-READ BUS CONTENTION
Figure 7



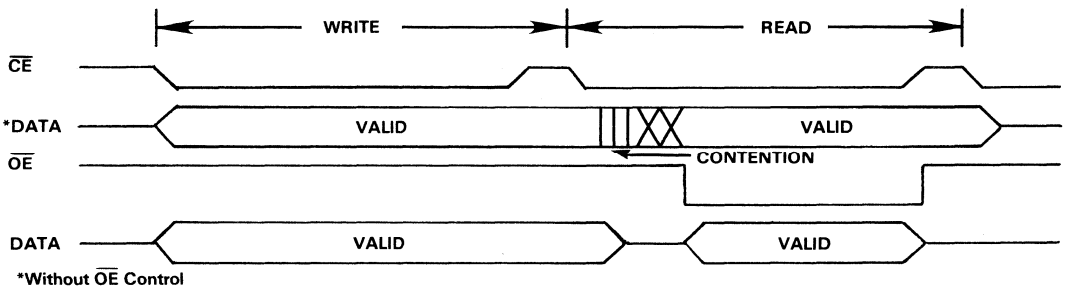
$\overline{CE}$ the potential exists for the buffer to turn on before the data in (write data) from the microprocessor goes high impedance. The addition of an $\overline{OE}$ control function would allow the selection and initialization of the read to occur without delay by using $\overline{OE}$ to gate the read data on the bus after the write data cleared the bus. Figure 8 shows what happens with and without the additional $\overline{OE}$ control.

An even more restrictive condition exists when the data bus is bidirectional and address is multiplexed as in the 8085 or 8086 microprocessor. In this case the read cycle first has an address on the bus followed by data, as shown in Figure 9.

With a sole $\overline{CE}$ control a fast memory could cause bus contention by sourcing or sinking output current before the bus achieved a high impedance condition from the address state. This contention problem can be resolved without performance degradation by the addition of an $\overline{OE}$ as seen in Figure 9.

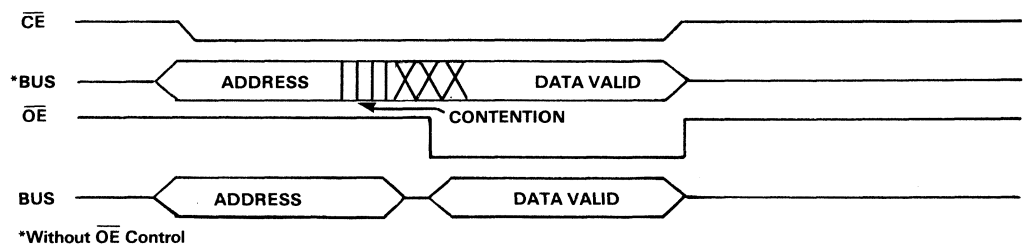
In short, the addition of the $\overline{OE}$ control function on Mostek's BYTEWYDE memories provides the designer with a powerful tool to resolve bus contention problems. Memories without two control functions often result in more restrictive performance or external bus control elements.

WRITE-READ BUS CONTENTION
Figure 8



*Without $\overline{OE}$ Control

ADDRESS-DATA BUS CONTENTION
Figure 9



*Without $\overline{OE}$ Control

INTERFACES TO POPULAR MICROPROCESSORS

Microprocessor applications have become pervasive. The ability to replace discrete hardware logic with microprocessor software has been closely coupled with advances in memory technology.

The spectrum ranges from consumer applications where cost and volume availability are paramount to the high performance and/or hi-reliability applications areas where cost is not the greatest concern. The consumer applications include video games, home computers, trip monitors, household controllers, etc.

BYTEWYDE memory has been designed to fit into those applications requiring full utilization of the microprocessor performance and low cost. It can quite easily be interfaced almost directly to any microprocessor. The Figures, Schematics, and Timing diagrams which follow illustrate this concept.

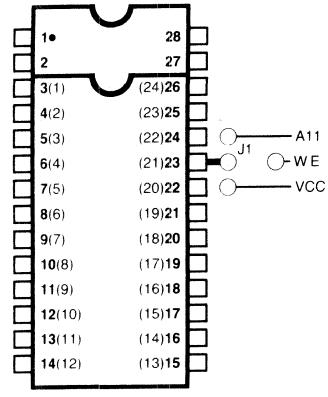
Figure 10 shows how the BYTEWYDE memory may be connected to the very popular present day 8 bit microprocessor MK3880 (Z80). This is a very simple configuration utilizing 28 pin sockets with the capability of using any RAM, ROM, or EPROM memory size. The high order microprocessor address bits are fed to a 74S387 256 x 4 PROM for address space decoding. The PROM allows the address space to be redefined at any time so that various mixes of RAM, ROM or EPROM can be used. The number of jumper connections required to utilize from 1K x 8 to 8K x 8 of PROM, 1K x 8 to 8K x 8 of

MOSTEK'S BYTEWYDE STATIC MEMORY FAMILY

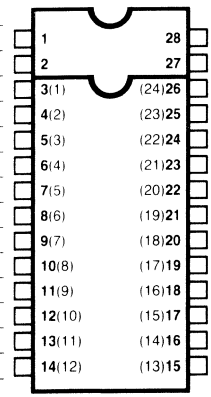
Table 1

Memory Type	Part Number	Capacity	Package	Jumper J1
ROM	MK34000	2K × 8	24 Pin	NC
ROM	MK37000	8K × 8	28 Pin	A11
ROM		32K × 8 △	28 Pin	A11
RAM	MK4802	2K × 8	24 Pin	WE
RAM		4K × 8 △	28 Pin	A11
RAM	MK4118A/4801A	1K × 8	24 Pin	WE
EPROM	MK2716	2K × 8	24 Pin	VCC
EPROM	MK2764 △	8K × 8	28 Pin	A11

△ available 1981



4118/A 4801A	4802	34000	2716	4K × 8	37000	32K × 8	2764
				NC	NC	A14	NC
				NC	A12	A12	A12
A7	A7	A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0	A0	A0
D0	D0	D0	D0	D0	D0	D0	D0
D1	D1	D1	D1	D1	D1	D1	D1
D2	D2	D2	D2	D2	D2	D2	D2
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS



2764	32K × 8	37000	4K × 8	2716	34000	4802	4118A 4801A
VCC	VCC	VCC	VCC				
NC	NC	NC	$\overline{WE}$				
NC	A13	NC	NC	VCC	VCC	VCC	VCC
A8	A8	A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9	A9	A9
A11	A11	A11	A11	VPP	NC	$\overline{WE}$	$\overline{WE}$
$\overline{OE}$ VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A/$\overline{O}$	A10	A/$\overline{O}$	A10	A10	A10	NC
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
D7	D7	D7	D7	D7	D7	D7	D7
D6	D6	D6	D6	D6	D6	D6	D6
D5	D5	D5	D5	D5	D5	D5	D5
D4	D4	D4	D4	D4	D4	D4	D4
D3	D3	D3	D3	D3	D3	D3	D3

Parenthesis Indicates Pin Number of 24 Pin Packages.
24 Pin Devices are Lower Justified in Pins 3 Thru 26 of 28 Pin Socket

MOSTEK'S BYTEWYDE STATIC MEMORY FAMILY

Table 2

Microprocessor	MK2716	MK37000	MK34000	MK4118A 4802	MK2764	Delay (2)
8085A 3Mhz Clock	-7	-5	-3	-4	TCE = 435	140
8085A-2 5 Mhz Clock	TCE = 270	-4	-3	-4	TCE = 270	80
8088 5Mhz Clock	-6	-5	-3	-4	TCE = 355	95
8086 5Mhz Clock	-6	-5	-3	-4	TCE = 355	95
MC6800 1.0Mhz Clock	-8	-5	-3	-4	-8	80
MC6802 1.0Mhz	-8	-5	-3	-4	-8	80
MC6809 1Mhz Clock	-8	-5	-3	-4	-8	95
MC68A09 1.5Mhz Clock	-5	-5	-3	-4	TCE = 345	95
MC68B09 2.0Mhz Clock	TCE = 245	-4	TCE = 245	-4	TCE = 245	75
6500 Series 1Mhz Clock	-6	-5	-3	-4	TCE = 355	75
MK3880 Z80 2.5Mhz Clock	-7	-5	-3	-4	TCE = 440	165
MK3880-4 Z80A 4Mhz Clock	TCE = 225	TCE = 225	TCE = 225	-4	TCE = 225	115
Z8002 4Mhz Clock	-5	-4	TCE = 300	-4	TCE = 300	100

NOTES 1. All μP clock speeds given are maximums allowed for each part or are stated fastest device in a series. By slowing clock speeds more flexibility in memory component selection is achieved.

2. Delay = time between μP valid address and chip enable time

EPROM and 1K x 8 to 8K x 8 of RAM, are few. The jumper connections and pin function comparisons are shown for various memory types and sizes in Table 1. The memory configuration can be expanded to 8 sockets by the addition of an extra 256 x 4 PROM address decoder. This combined with the 28 pin socket concept allows the memory to be upgraded to the 64K x 8 level as higher density memories become available.

The control functions are also very simple as shown. $\overline{WR}$ goes directly to $\overline{WE}$, $\overline{RD}$ goes to $\overline{OE}$ and $\overline{MREQ}$ is connected to the enable on the **74S387** PROM.

Figure 11 shows a typical connection possibility for BYTEWYDE Memory to a Motorola 6809 microprocessor. The control signals in this case require some extra logic before being connected to the memory. There are basically two reasons for this extra logic requirement. One is due to the fact that on the 6809, the R/$\overline{W}$ controls are on the same pin. Some logic is needed to generate $\overline{OE}$ and $\overline{WE}$ signals.

The second reason is a combination of items. Mostek's BYTEWYDE RAMs require that data inputs be held valid after the trailing edge of $\overline{WE}$. In the 6809 data goes away at the same time as R/$\overline{W}$. The extra logic shown in Figure 11 uses the clock E and quadrature clock Q to take $\overline{WE}$ high prior to the 6809 taking R/$\overline{W}$ high. This insures that $\overline{WE}$ goes high approximately one quarter cycle prior to data input going away.

In order to use the Edge Activated™ 64K ROM, E and Q are also used to enable the PROM decoder. This provides both an active period of ¾ of the μprocessor cycle and ¼ of a period for $\overline{CE}$ precharge as required by "Edge Activated"™ devices. All other connections to the 6809 are the same as in the MK3880.

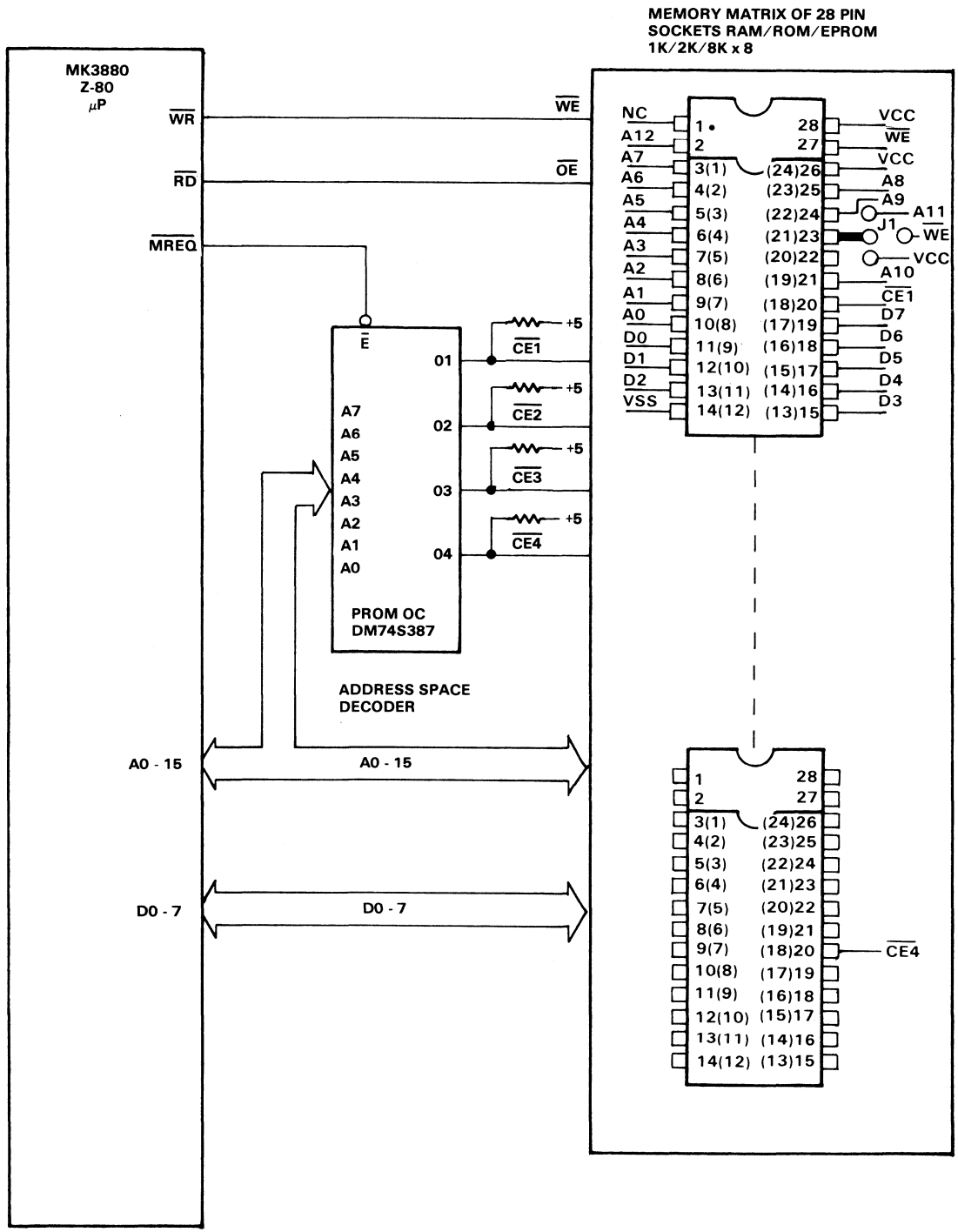
The Intel 8085/8088 (Figure 12) provides another unique situation, however again the BYTEWYDE fits quite easily. Read and write controls connect directly as in the 3880 μP. Two microprocessor signals that require looking at are IO/$\overline{M}$ and ALE. The IO/$\overline{M}$ signal is used to determine whether data will be to or from an I/O device or memory. ALE is the address latch enable signal used to clock addresses into the latch so that the pins can be used for data since the 8085/8088 has common data and address lines. Therefore, IO/$\overline{M}$ and ALE are connected to the $\overline{Enable}$ and Enable respectively of the PROM decoder.

One of the new generation 16 bit microprocessors, the Intel 8086, is shown configured to the BYTEWYDE memory. The connections are the same as in the 8085 except in this case two BYTEWYDE Memories are required to handle 16 bits of data. Two PROM decoders are required to generate the $\overline{CE}$ ($\overline{CS}$) signals in order to meet the byte addressability requirements. The 8086 can pick either 8 or 16 bits at a time. Otherwise one decode would suffice.

Also included in Figure 13 thru 16 are examples to interface with such popular microprocessors as the 6500, 6800, 8086, Z80 and Z-8000. Table 2 identifies the specific dash number required for each memory type to microprocessor performance characteristics.

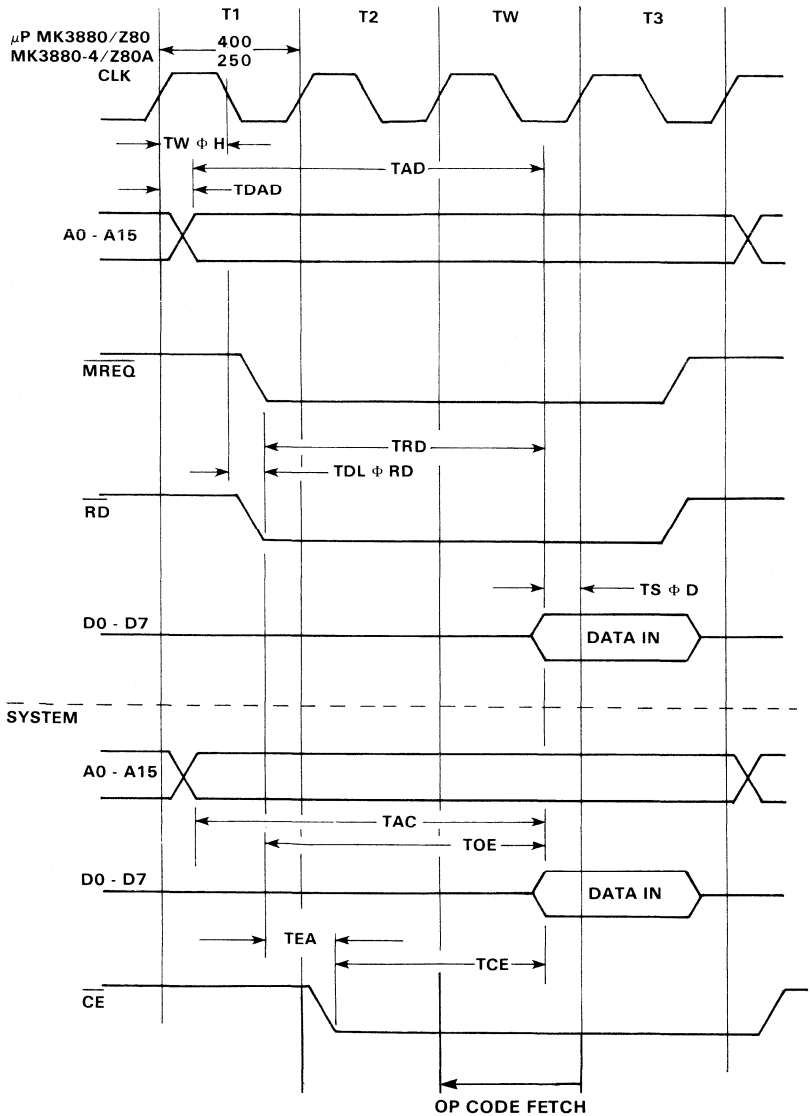
INTERFACE TO 3880/Z80

Figure 10



INTERFACE TO 3880/Z80

Figure 10a



μP MK3880

TC = T1 = 400 TAD = (T1-TDAD) + (T2-TSΦD)
TDAD = 145 TAD = 255 + 350 = 605
TSΦD = 50 TRD = T1 -(TWΦH + TDLΦRD) + (T2-TSΦD)
TWΦH = 180 TRD = 120 + 350 = 470
TDLΦRD = 100

SYSTEM

TAC = AVAILABLE FOR ADDRESS ACCESS = TAD
TAC = 605
TCE = AVAILABLE FOR CHIP SELECT = TRD-TEA[1]
TCE = 440
TOE = AVAILABLE FOR MEMORY = TRD
TOE = 470

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

μP MK3880-4

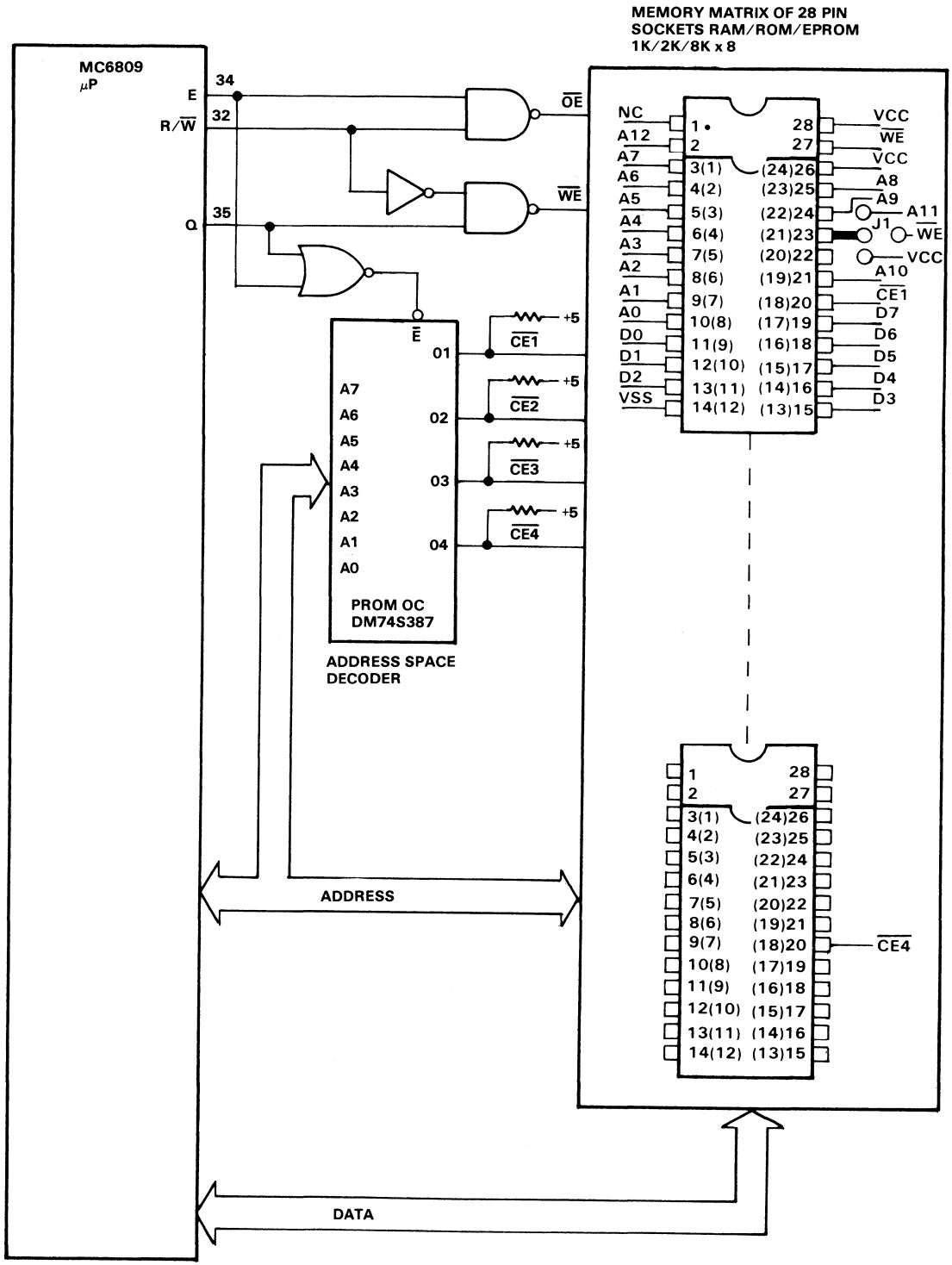
TC = 250 TAD = 340
TDAD = 110 TRD = 255
TSΦD = 50
TWΦH = 110
TDLΦRD = 85

SYSTEM

TAC = 340
TCE = 225
TOE = 255

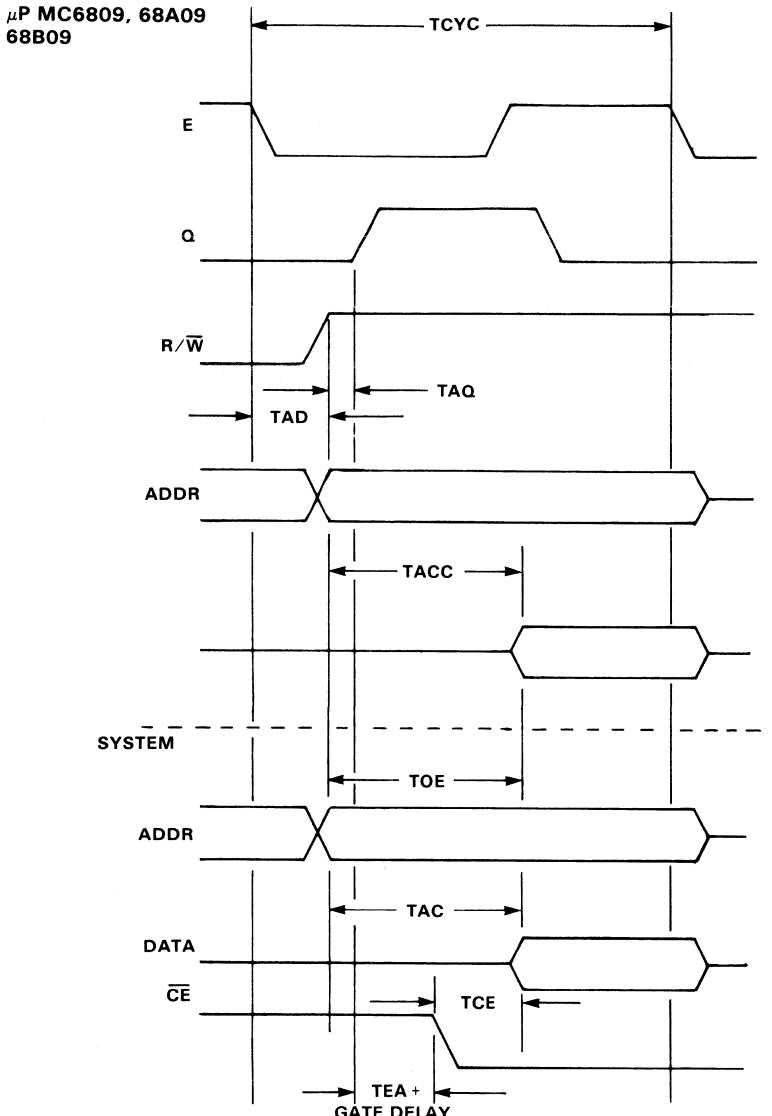
INTERFACE TO 6809

Figure 11



INTERFACE TO 6809

Figure 11a



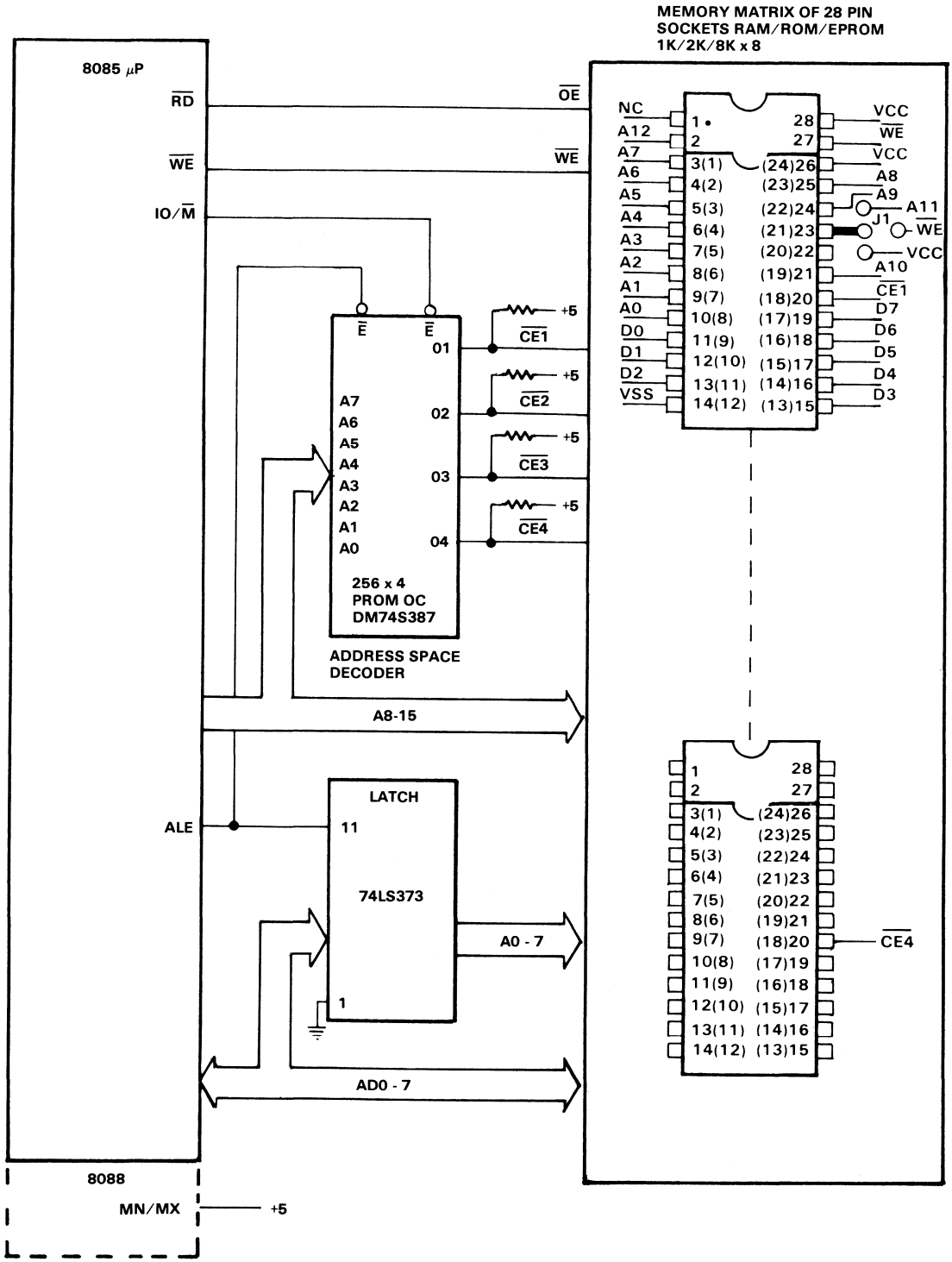
μP6809	SYSTEM
TACC = 695	TAC = AVAILABLE FOR ADDRESS = TACC
TAD = 200	TAC = 695
TAQ = 50	TCE = AVAILABLE FOR CHIP SELECT = TACC-TAQ-(TEA[1] + GATE DELAY)
TCYC = 1000	TCE = 695-50-45
	TCE = 600
	TOE = AVAILABLE FOR MEMORY = TACC
	TOE = 695

μP68A09	SYSTEM
TACC = 440	TAC = 440
TAD = 140	TCE = 345
TAQ = 50	TOE = 440
TCYC = 667	

μP68B09	SYSTEM
TACC = 320	TAC = 320
TAD = 110	TCE = 245
TAQ = 30	TOE = 320
TCYC = 500	

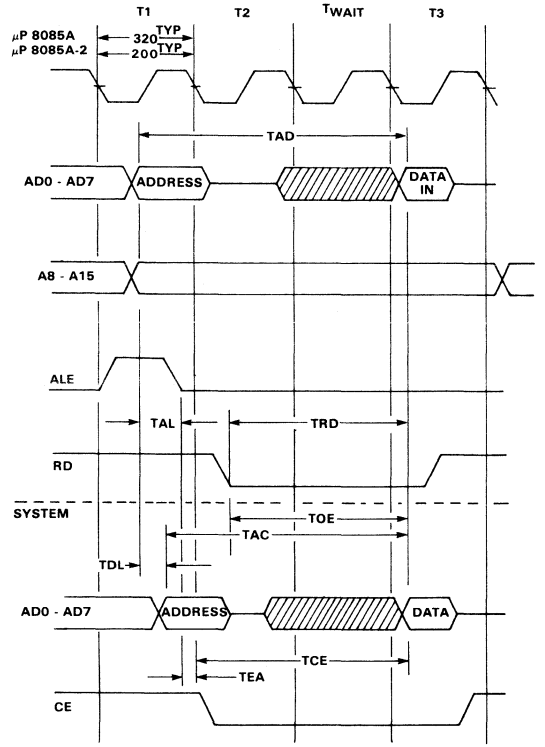
NOTE 1 TEA = ENABLE ACCESS TIME of DM74S387

INTERFACE TO 8085/8088
Figure 12



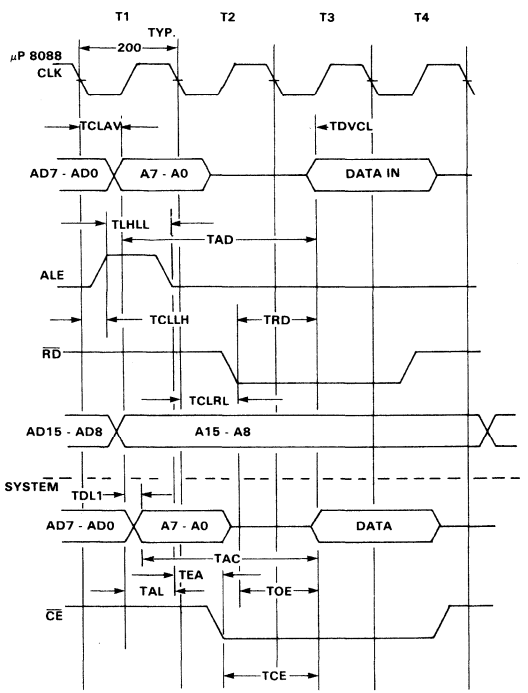
INTERFACE TO 8085

Figure 12a



μP8085A	SYSTEM
TAD = 575	TAC = AVAILABLE FOR ADDRESS ACCESS = TAD-TDL
TRD = 300	TAC = TAD (μP)-74LS373 DELAY
TAL = 110	TAC = 575-15 = 560
	TCE = AVAILABLE FOR CHIP SELECT
	TCE = TAD (μP)-TAL - TEA (ENABLE ACCESS OF DM74S387)
	TCE = 575-140 = 435
	TOE = AVAILABLE FOR MEMORY = TRD
	TOE = 300

μP8085A-2	SYSTEM
TAD = 350	TAC = AVAILABLE FOR ADDRESS = TAD-TDL
TRD = 150	TAC = TAD (μP)-74LS373 DELAY
TAL = 50	TAC = 350-15 = 335
	TCE = AVAILABLE FOR CHIP SELECT
	TCE = TAD (μP)-TAL-TEA (ENABLE ACCESS OF DM74S387)
	TCE = 350-80 = 270
	TOE = AVAILABLE FOR MEMORY = TRD
	TOE = 150



μP 8088

TCLAV = 110	TAD = (TI-TCLAV) + T2+ (T3-TDVCL)
TDVCL = 30	TAD = (200-110) + 200 + (200-30)
TCLLH = 80	TAD = 460
TLHLL = 105	TAL = TCLLH + TLHLL - TCLAV = 75
TCLRL = 10	TRD = (T2-TCLRL) + (T3-TDVCL)
	TRD = (200-165) + (200-30)
	TRD = 205

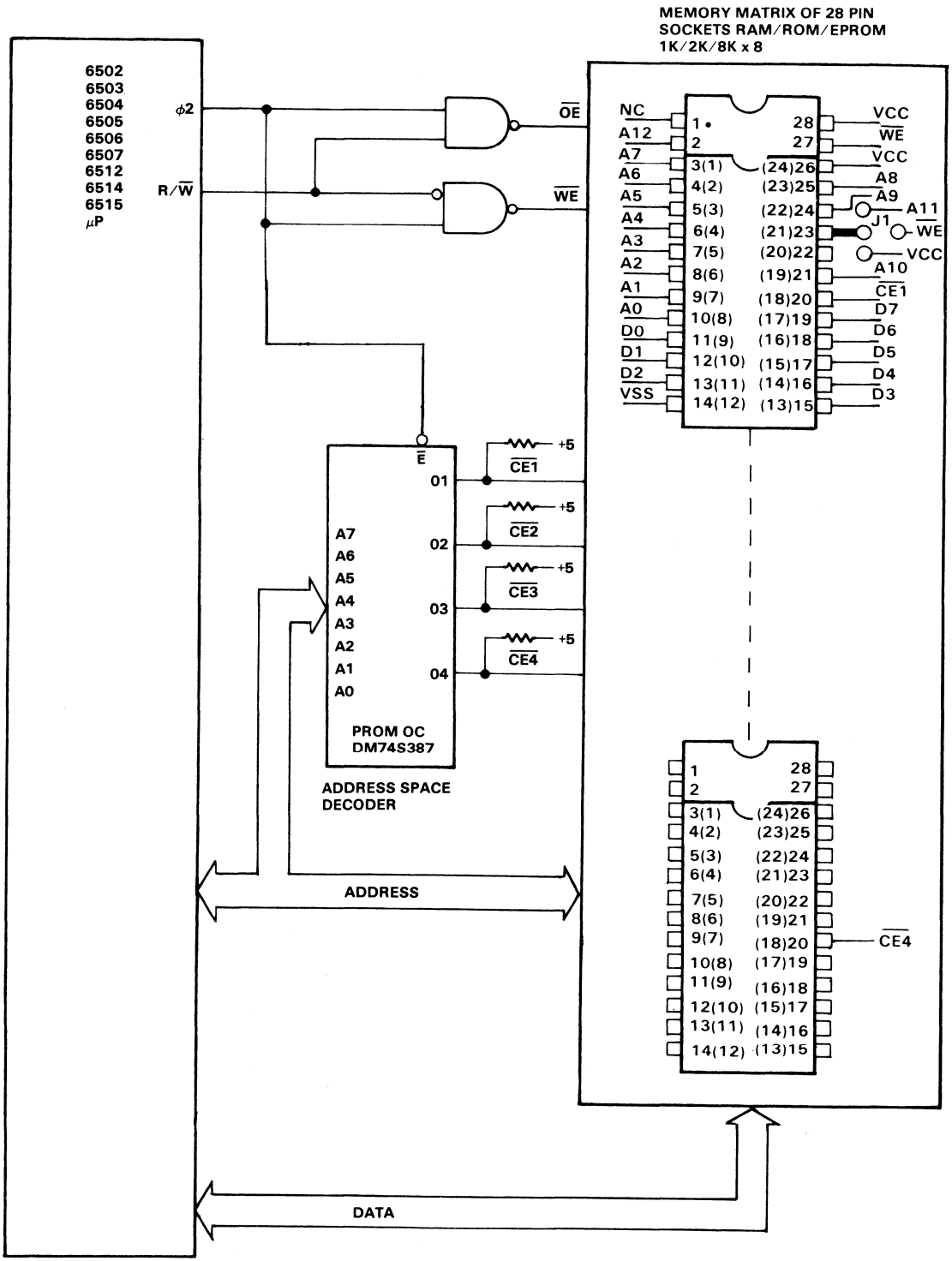
SYSTEM

TAC = AVAILABLE FOR ADDRESS ACCESS = TAD-TDL1
TAC = TAD μP -74LS373 DELAY
TAC = 460-18 = 442
TCE = AVAILABLE FOR CHIP SELECT = TAD-TAL-TEA[1]
TCE = 460-75-30 = 355
TOE = AVAILABLE FOR MEMORY = TRD
TOE = 205

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

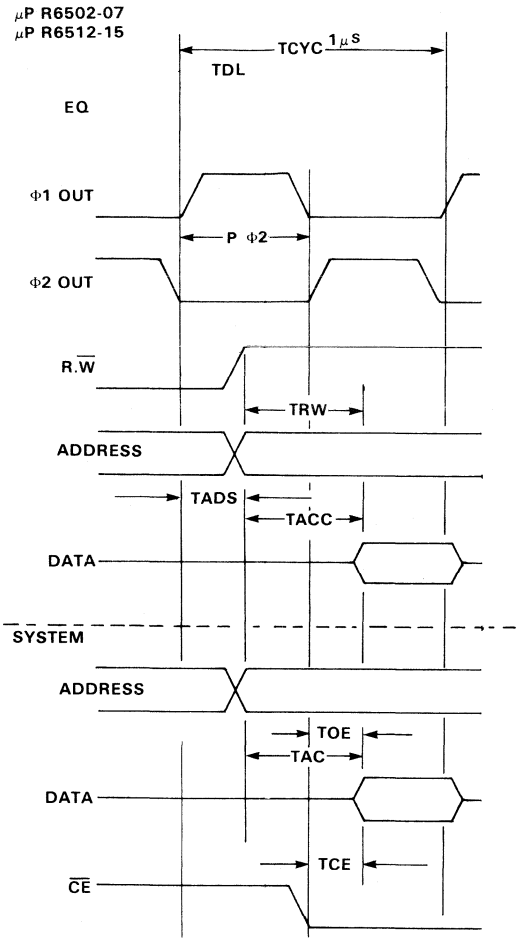
INTERFACE TO 6500

Figure 13



INTEFACE TO 6500

Figure 13a

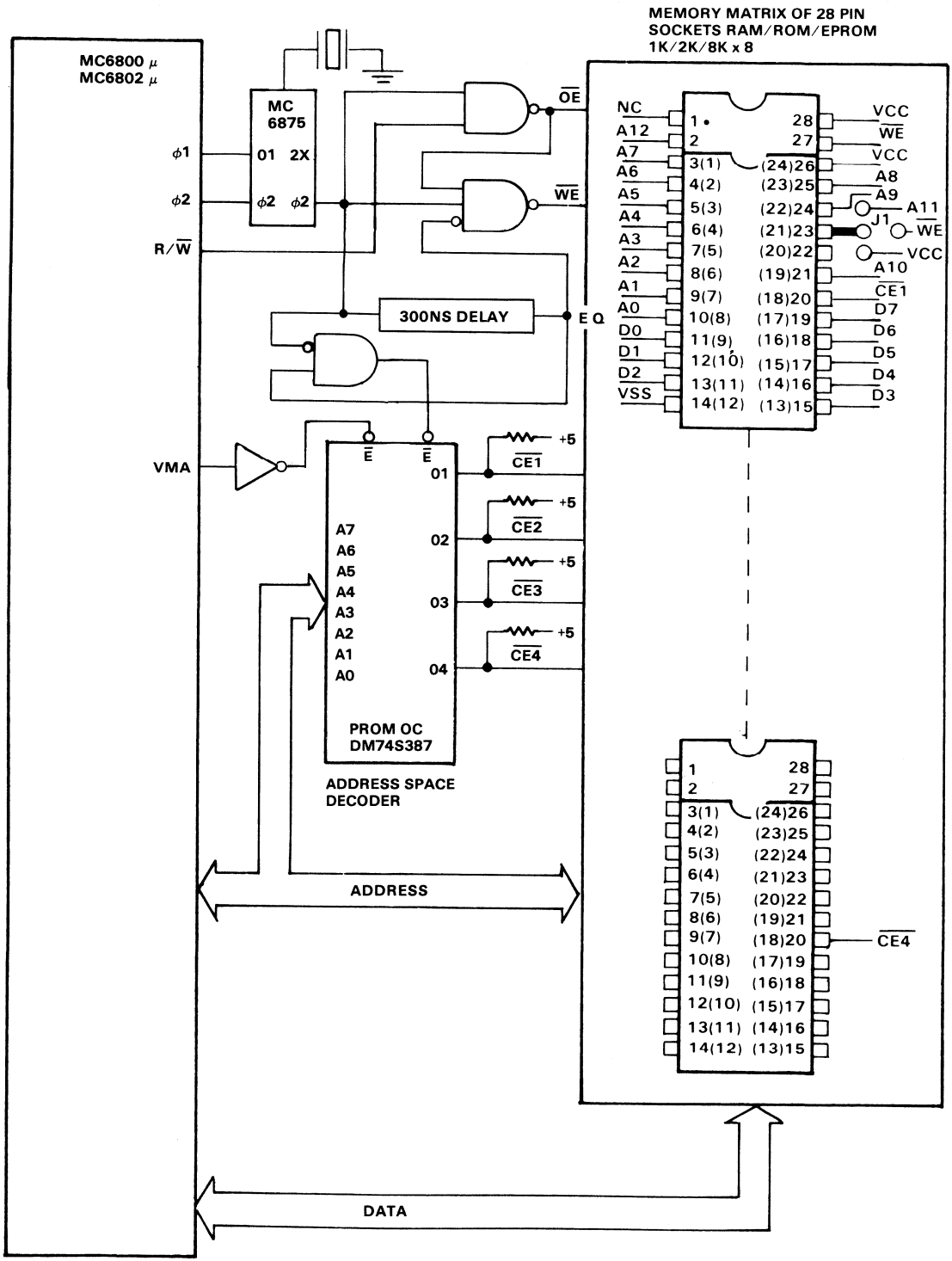


μP 6500 SERIES	SYSTEM
TACC = 650	TAC = AVAILABLE FOR ADDRESS = TACC
TRW = 650	TAC = 650
PΦ2 = 500	TCE = AVAILABLE FOR CHIP SELECT = TADS + TACC -(PΦ2 + GATE DELAY)
TADS = 225	TCE = 225 + 650 -(500 + 20)
TDL = 250	TCE = 355
	TOE = AVAILABLE FOR MEMORY = TACC + TADS - (PΦ2+ GATE DELAY)
	TOE = 650 + 225 - 520
	TOE = 255

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

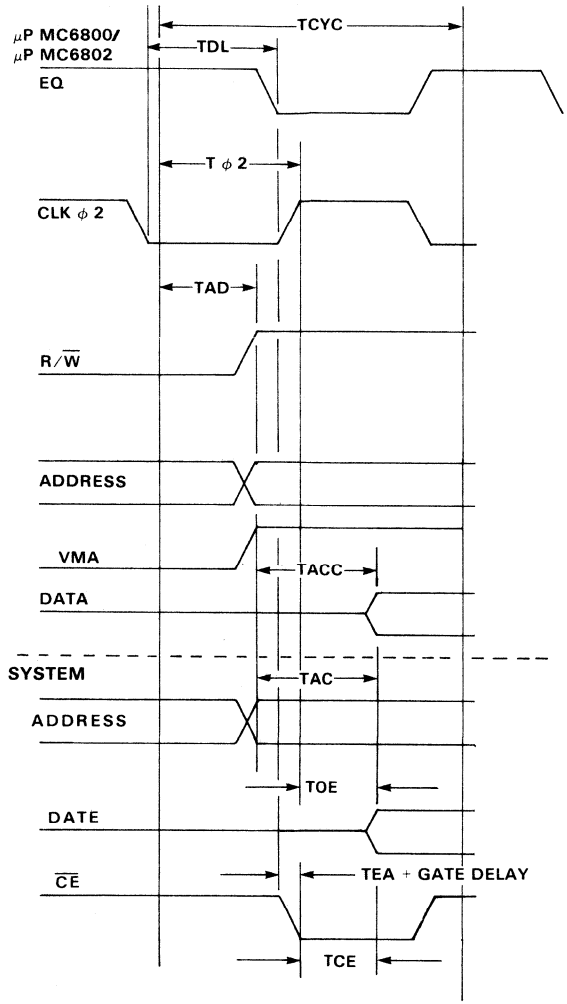
INTERFACE TO 6800

Figure 14



INTERFACE TO 6800

Figure 14a



μP MC6800
μP MC6802

TCYC = 1μS
TAD = 270
TACC = 530
Tφ2 = 500
TDL = DELAY LINE = 300ns USING DELAY LINE OR ONE SHOT

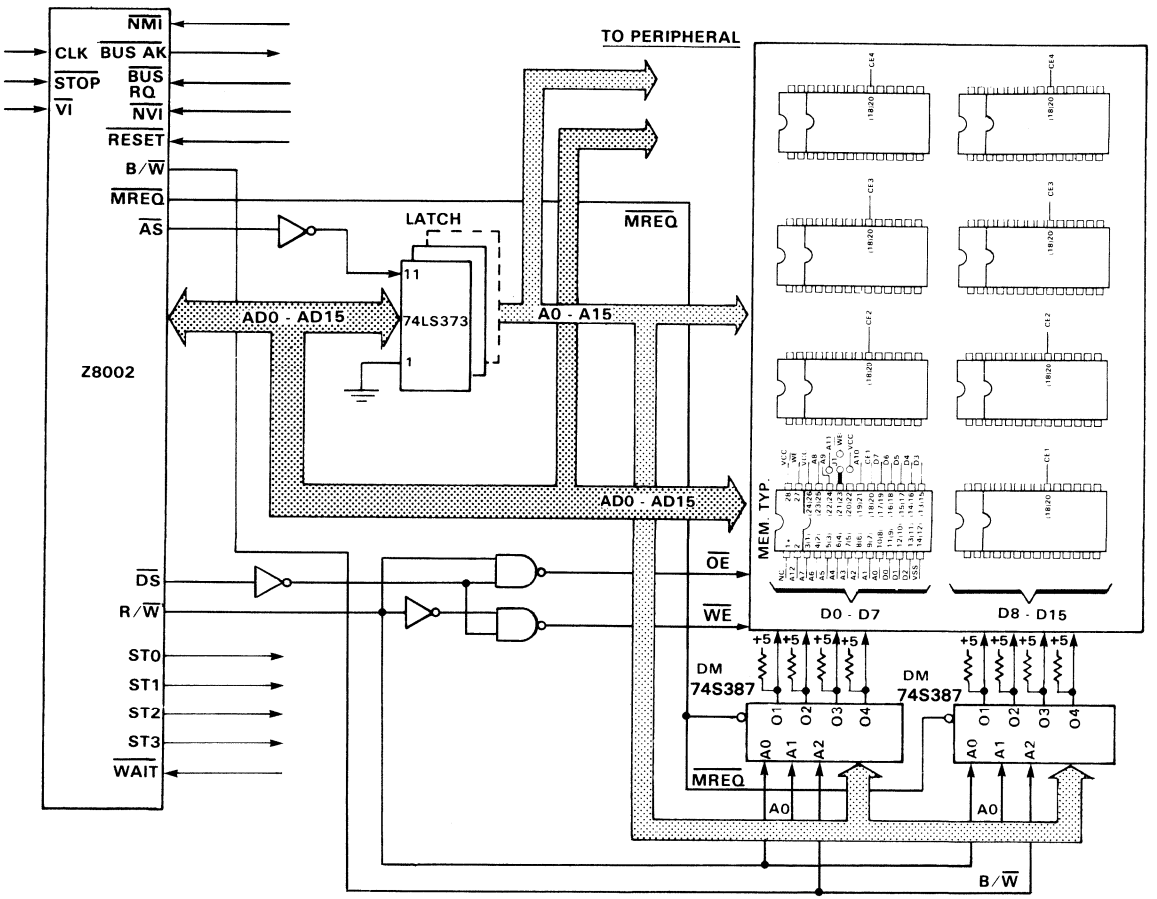
SYSTEM

TAC =AVAILABLE FOR ADDRESS ACCESS = TACC
TAC = 530
TCE = AVAILABLE FOR CHIP SELECT = TACC - (TDL - TAD) - (TEA + GATE DELAY)
TCE = 530 - 30 - (30 + 20) = 450
TOE = AVAILABLE FOR MEMORY = TACC - (Tφ2 - TAD) - GATE DELAY
TOE = 255

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

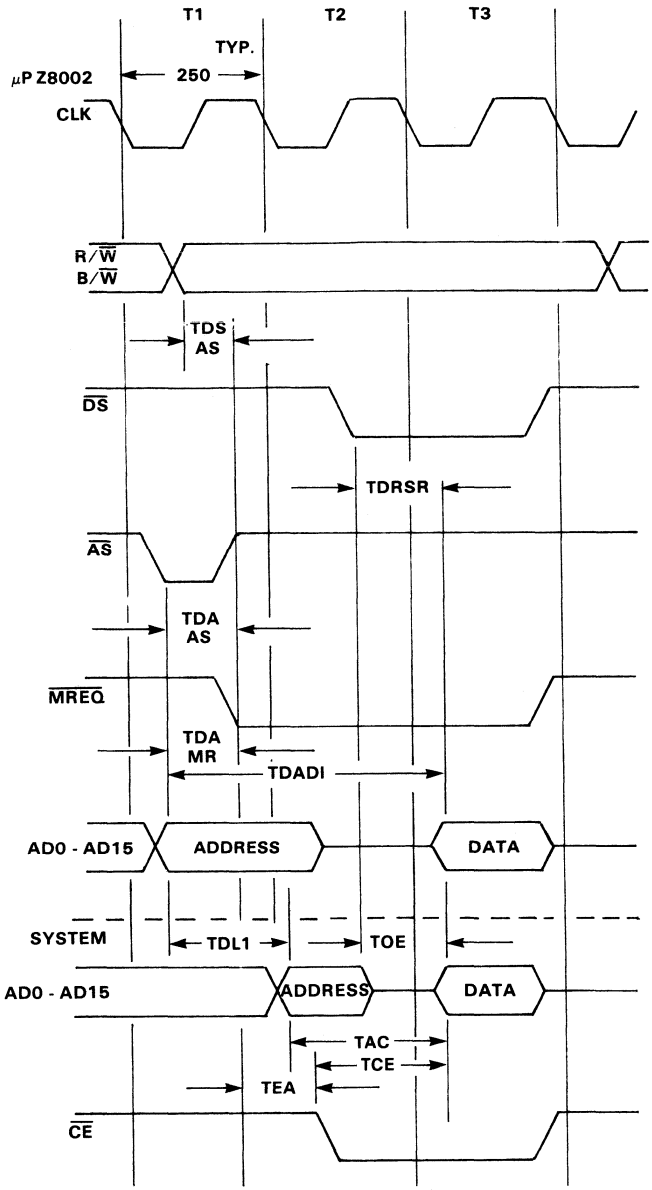
INTERFACE TO Z8000

Figure 15



INTERFACE TO Z8000

Figure 15a



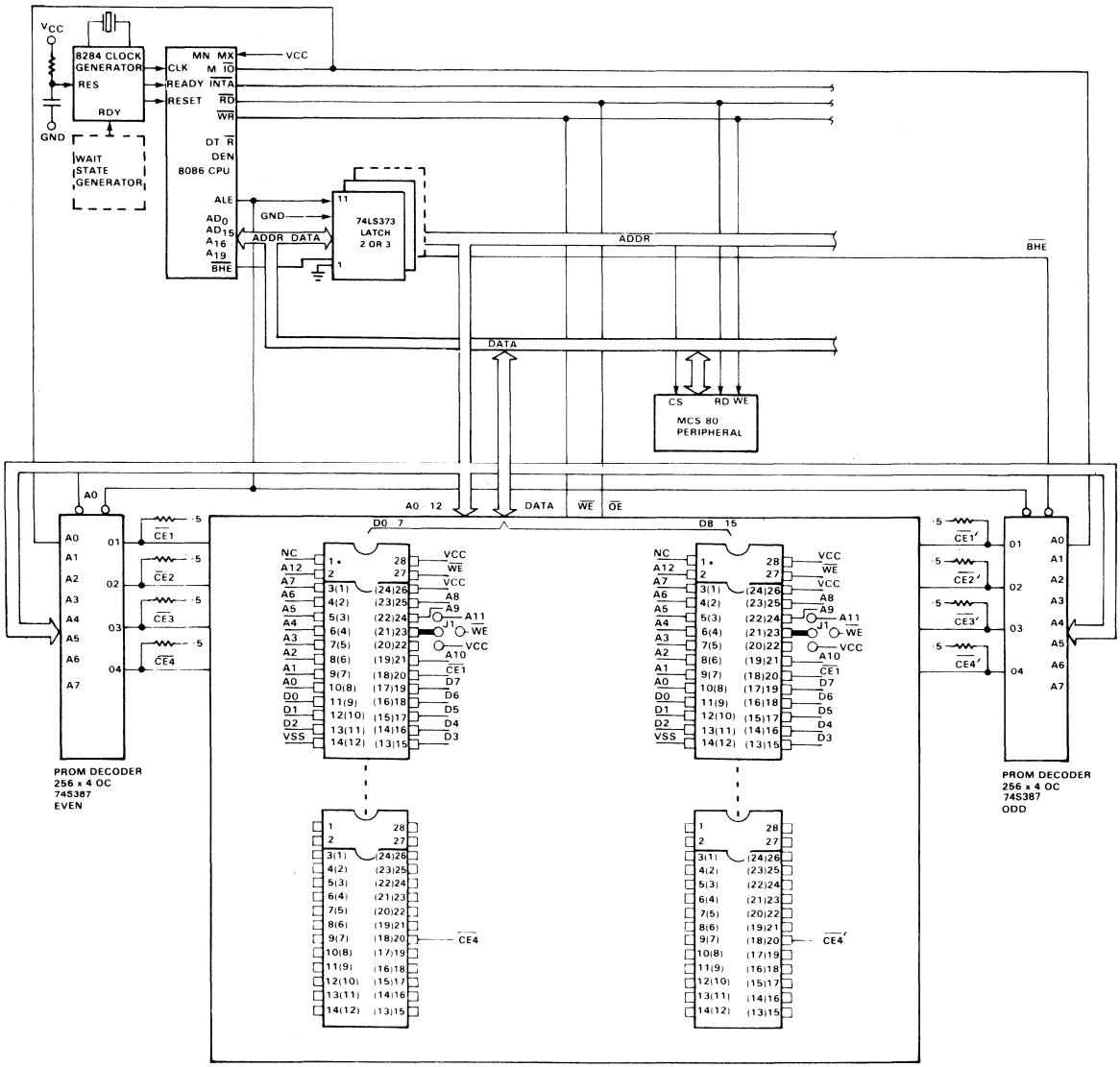
μPZ8002
TDADI = 400
TDAMR = 70
TDDSR = 155

SYSTEM
TAC = AVAILABLE FOR ADDRESS ACCESS
TAC = TDADI - TDL1
TAC = TDADI-(-74LS373 DELAY)
TAC = 400 - (18)
TAC = 382
TCE = AVAILABLE FOR CHIP SELECT
TCE = TDADI-(TDAMR + TEA[1])
TCE = 400-100
TCE = 300
TOE = AVAILABLE FOR MEMORY
TOE = TDDSR
TOE = 155

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

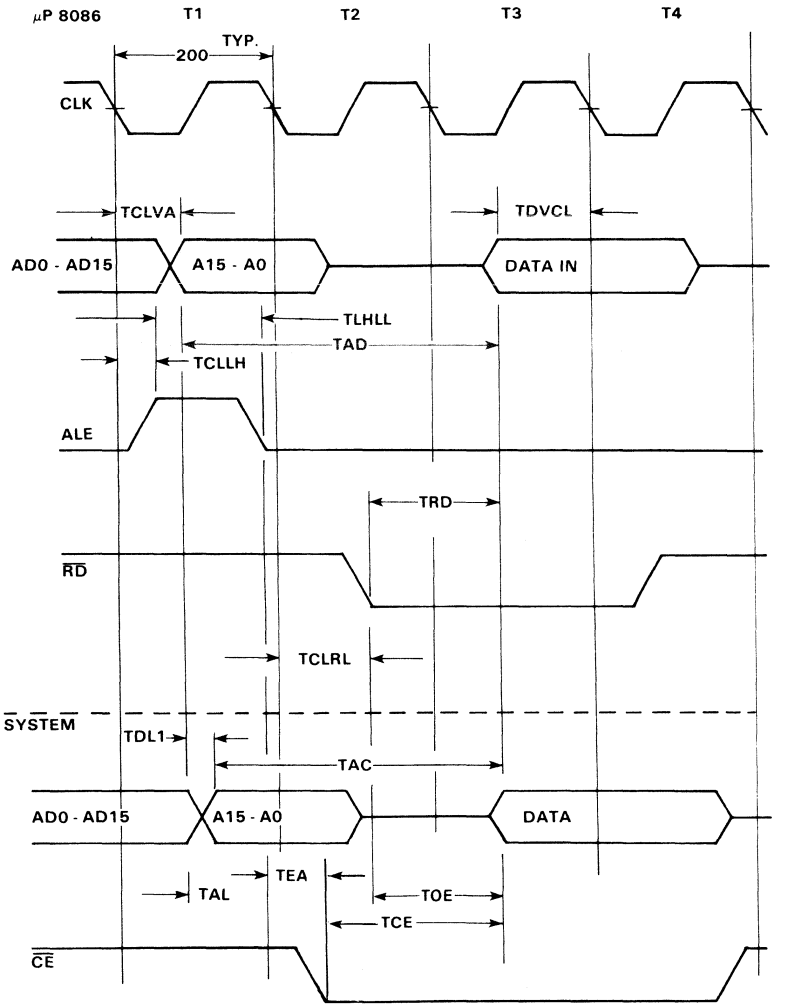
INTERFACE TO 8086

Figure 16



INTERFACE TO 8086

Figure 16a



μP 8086

TLHLL = 105	TAD = (TI-TCLAV) + T2 + (T3-TDVCL)
TCLAV = 110	TAD = (200-110) + 200 + (200-30)
TCLLH = 80	TAD = 460
TDVCL = 30	TAL = (TCLLH + TLHLL) -TCLAV = 75
TCLRL = 165	TRD = (T2-TCLRL) + (T3-TDVCL)
	TRD = (200 -165) + (200-30)
	TRD = 205

SYSTEM

TAC = AVAILABLE FOR ADDRESS ACCESS = TAD-TDL1
TAC = TAD(μP)-(74LS373)
TAC = 460-18 = 442
TCE = AVAILABLE FOR CHIP SELECT = TAD-TAL-TEA[1]
TCE = 355

TOE = AVAILABLE FOR MEMORY = TRD
TOE = 205

NOTE 1 TEA = ENABLE ACCESS TIME OF DM74S387

BYTEWYDE PRINTED CIRCUIT BOARD EXAMPLE

A printed circuit board layout using Mostek's BYTEWYDE Static Memory was designed to illustrate the density and flexibility of the BYTEWYDE approach. This layout is universal i.e., ROM/EPROM/RAM, 8 bit or 16 bit. A particular system may not require an all-encompassing design so simplifications are possible while still maintaining design and PC board flexibility. This design supports the following features:

1. 24/28 pin socket sites for present and future devices
2. Individual socket jumpers to support RAM/ROM/EPROM interchange
3. Programmable address space decoder to support 1K/2K/4K/8K Byte Address space for each socket
4. Modular expansion in four socket increments
5. 8 bit or 16 bit data words
6. Two sided printed circuit board layout rules

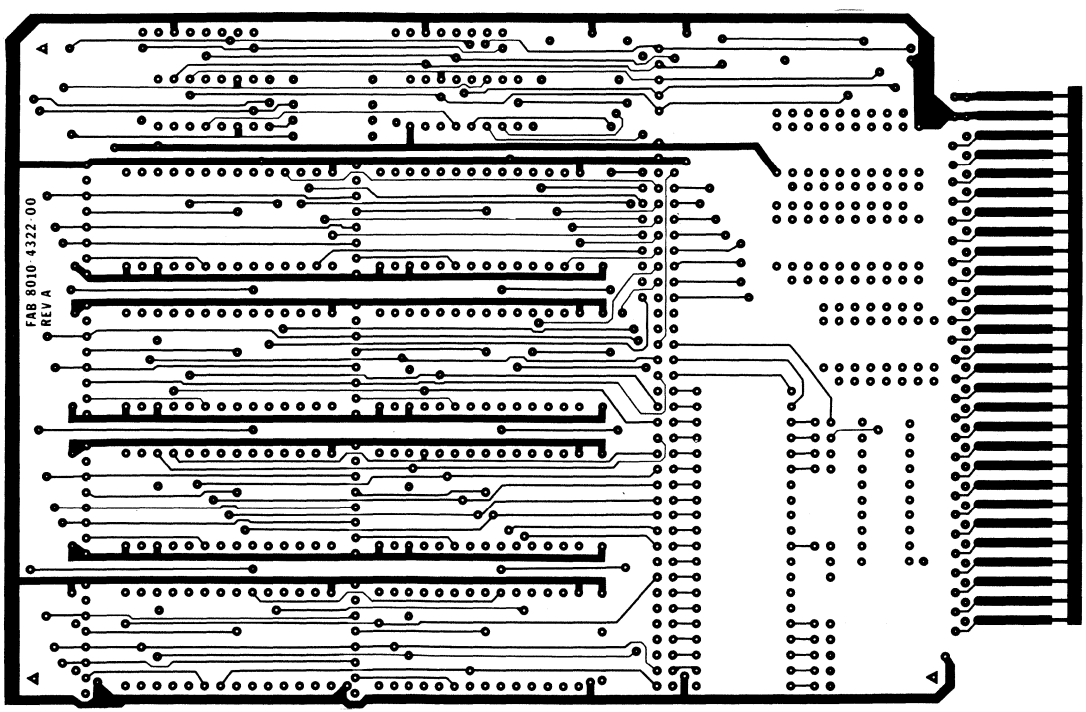
Since microprocessors are well suited to this design philosophy provisions were incorporated on the printed circuit boards for a 40 pin microprocessor socket. Additional 16 and 20 pin socket sites are available to provide the latches and gates sometimes necessary to support the processor memory interface. Figure 19 is a schematic diagram of memory interfaced to the MK3880 microprocessor.

The BYTEWYDE Memory Board is a 2 x 4 array using 28 pin sockets (U0 - U7). By lower justifying 24 pin BYTEWYDE memories, today's product can be used. By having 28 pin sockets new generations of BYTEWYDE memories can replace the 24 pin devices without redesigning the memory board.

The BYTEWYDE board has ten (8 ea.) pin jumper locations. These occupy very little space while offering a great deal of flexibility. Jumper strips (J0 - J7) are located at the top of each memory socket. These stripes are for the different functions required of pins 21 and 23 in the memory array. Referring to the Mostek BYTEWYDE Static Memory Family Chart, pin 21 is for partials and 23 for ROM/RAM compatibility. Providing a jumper at each memory location allows any Mostek memory on this chart to be used in any of the 8 memory locations.

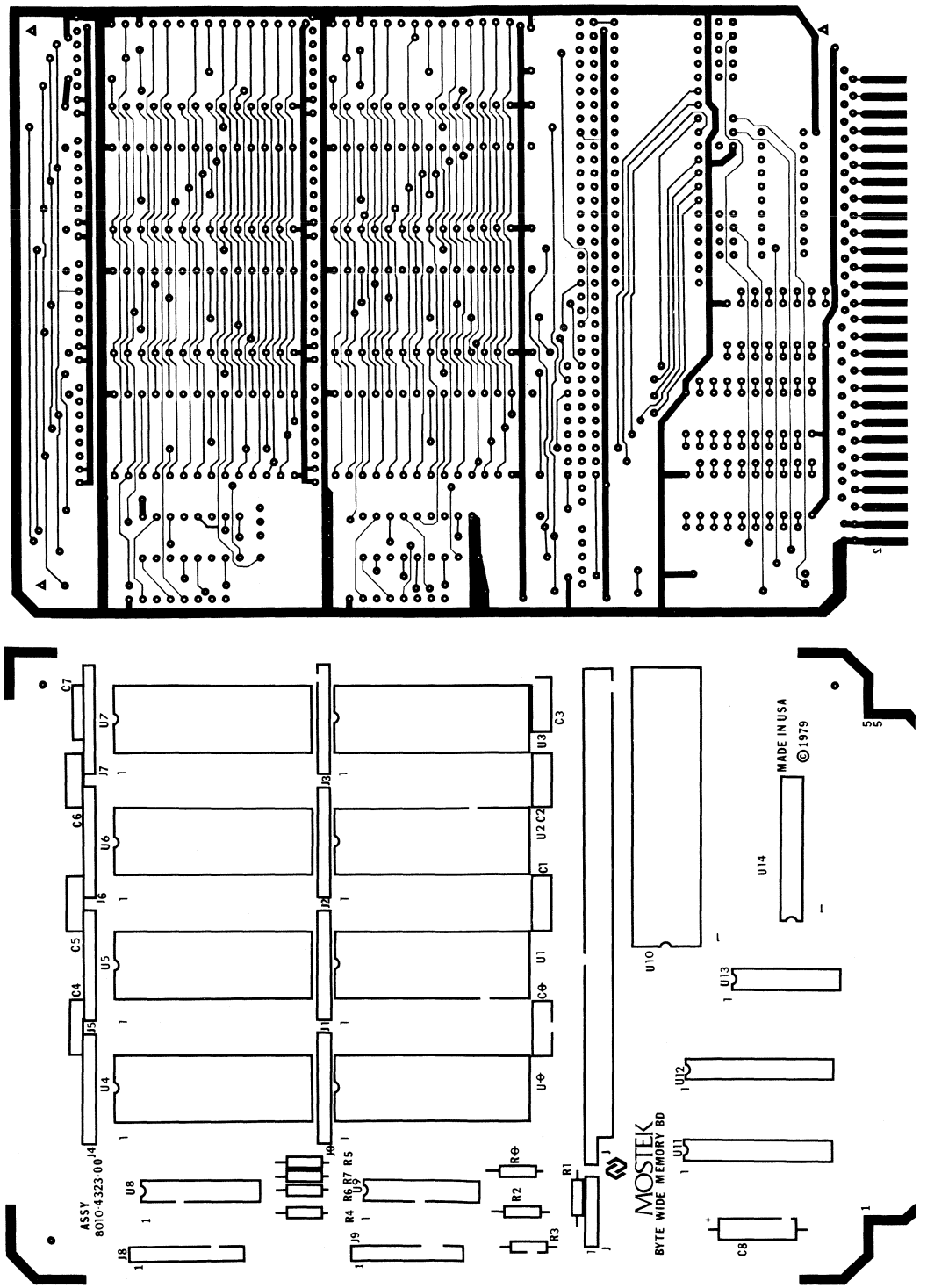
For decoding the memory array (2) 256 x 4 bipolar PROMs (U8 & U9) are used. Having two of these PROMs increases the flexibility of this board by allowing a 16 bit

PRINTED BOARD LAYOUT (SOLDER SIDE)
Figure 17



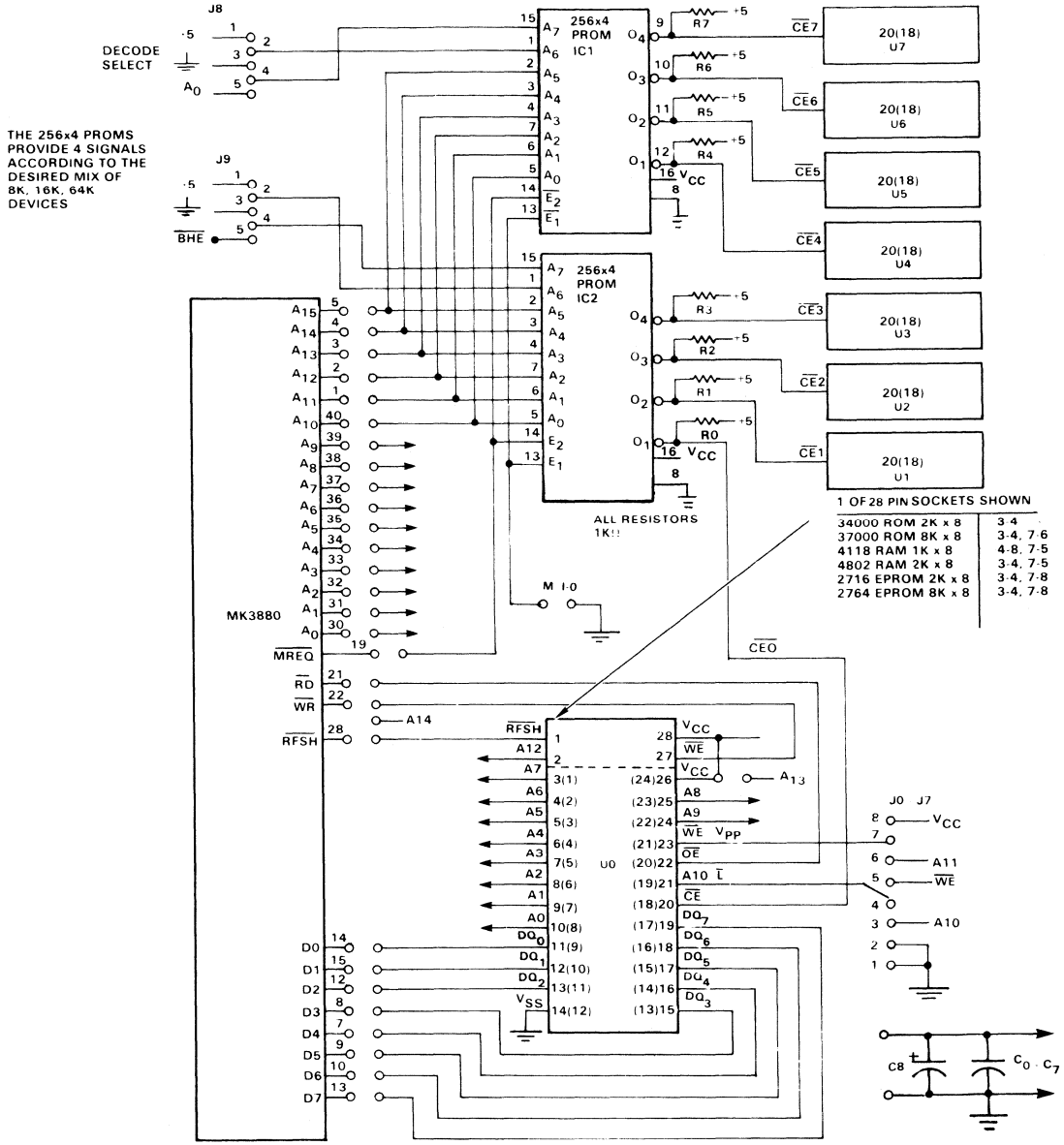
CIRCUIT BOARD LAYOUT (COMPONENT SIDE)

Figure 18



8K/16K/64/RAM/EPROM/ROM COMPATIBLE SOCKETS WITH MK3880

Figure 19



BYTEWYDE MEMORY BOARD PARTS LIST

Table 3

Units	Designator	Description
1 ea.	P.C. Board	BYTEWYDE Memory Board
8 ea.	U0 - U7	28 pin memory sockets
8 ea.	C0 - C7	**.1 μf, 25V decoupling capacitors**
8 ea.	J0 - J7	8 pin jumper connectors for each memory location
8 ea.	R0 - R7	1K Ω 5% resistors ¼ W
2 ea.	U8 & U9	16 pin sockets for PROMs
2 ea.	J8 & J9	8 pin jumper connections for PROMs
1 ea.	U10	40 pin socket for microprocessor
4 ea.	U11 - U14	μP interfacing sockets
1 ea.	C8	15μf, 15V electrolytic capacitor

microprocessor to interface to the memory array. Added versatility is made via the 2 jumper strips (J8 & J9). These strips allow use of the A0 address and $\overline{BHE}$ signal for the odd and even bytes which are needed by a 16 bit μP. The data lines coming from the array are split into two groups, the upper array and lower; therefore, the D0 - D7 and D8 - D15 distinction.

The 40 pin socket location is for the microprocessor. The Mostek 3880 μP can most easily be wired, but any μP can be used because of the universality which has been built into this board.

Four locations have been designated to generate gating, timing, and latching requirements for certain μP's. These locations are intended to be wire wrap sockets.

For more details on how to design a memory array for flexibility and expandibility without redesigning your memory each time, contact your Mostek Field Applications Engineer.

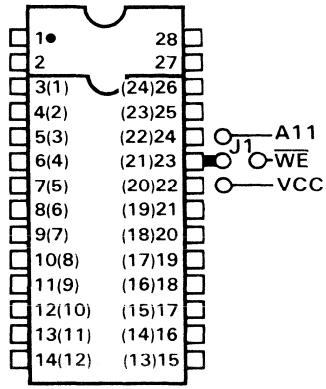
MICROPROCESSOR MEMORY ALTERNATIVES

Implementing microprocessor memory designs with a coherent packaging strategy enhances density. Mostek's BYTEWYDE Static Memory Family of RAM, ROM and EPROM make possible high density memory, yet allow for flexibility and future expansion. The commonly used approaches to build microprocessor memory are restrictive in that ROM and RAM do not share the same package.

Most microprocessor based systems require a portion of their memory to be nonvolatile, namely ROM. The exact mixture of ROM and RAM is rarely known at design time and frequently changes during the course of the product life. A substantial amount of the p.c. board space is conserved with a single matrix of 24/28 pin packages is designed, as opposed to the two matrixes, each having their own spare requirements for expansion.

Memory designs normally allow for memory expansion by providing spare sockets in the memory matrix. If RAM is chosen to be packaged and pin incompatible with ROM then two memory matrixes are required, each with their own expansion spare sockets. Given that exact requirements are rarely known at design time, this results in excessive unused p.c. board real estate because each matrix has it's own expansion requirements. An alternative is to choose a RAM which

JUMPER LAYOUT FOR MEMORY
Figure 20



is upgradable and plug compatible with ROM. In this way, a single memory matrix can be layed out. RAM and ROM can be mixed at will, causing fewer constraints to be placed on the memory configuration.

The Mostek MK4118 1K x 8 RAM is pin compatible with MK2716 2K x 8 EPROM and MK34000 2K x 8 ROM. Expansion can be accomplished by using the next generation higher density components which will be pin compatible with presently available BYTEWYDE memory.

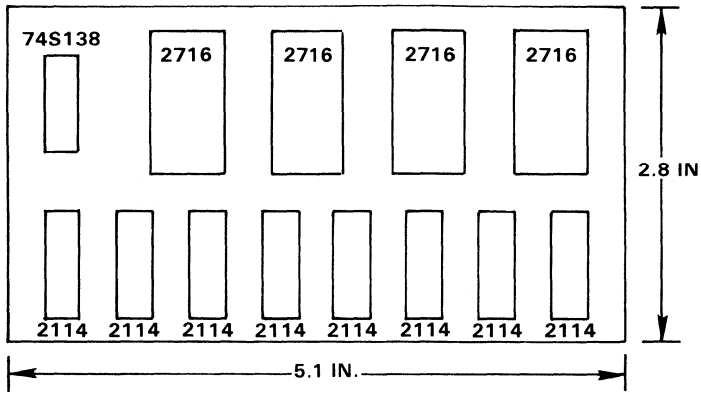
Density has and will continue to be an important criteria used to evaluate memory component selection. The two most popular microprocessor RAMs today are the 4118 1K x 8 and the 2114 1K x 4. The printed circuit board space requirement for the 1K x 8 of memory using 4118 is the same as using (2) 2114. However, the 2114 lacks ROM/EPROM compatibility and the 2114 cannot be expanded in density without package redesign. The 4118 will have a double density pin compatible upgrade 4802. The 4802 2K x 8 will be four times the density of the 2114 and requires half the board real estate.

A comparative analysis of current technology alternatives for implementing 4K x 8 RAM plus 8K x 8 EPROM memory has been performed. The printed circuit board density has been determined using 2 sided p.c. board layout rules. The advantages and disadvantages of each approach are summarized in a Table 4 and Figure 21.

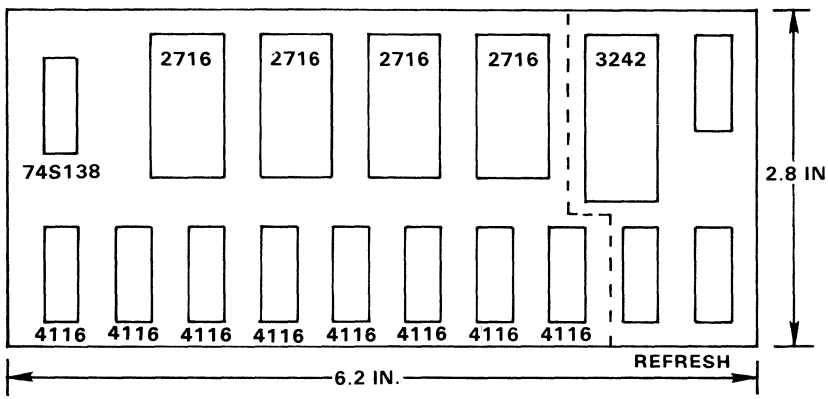
BOARD LAYOUT SPACE COMPARISONS

Figure 21

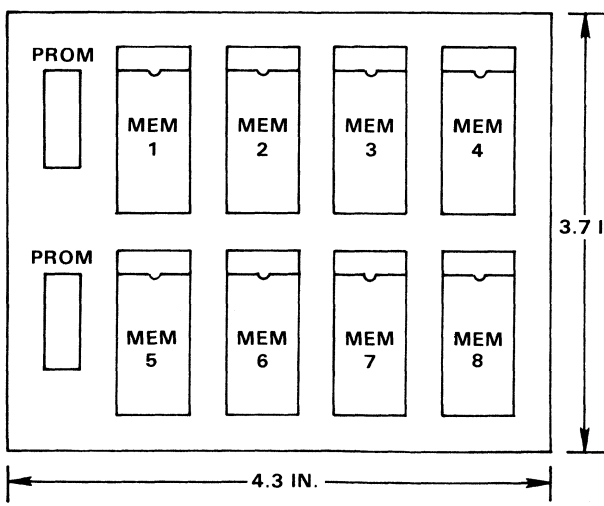
DUAL MATRIX A = 14.28 IN²



DUAL MATRIX B = 17.36 IN²



SINGLE MATRIX C = 15.91 IN²



COMPARATIVE ANALYSIS TABLE
Table 4

	Matrix A	Matrix B	Matrix C
Operation	Static	Dynamic	Static
RAM-ROM/PROM Mixture	Fixed at Design	Fixed at Design	Flexible-Any Mixture
Incremental RAM Expansion	1K Bytes	16K Bytes	1K Bytes
EPROM Upgrade	2732 (4K x 8)	2732 (4K x 8)	2732 (4K x 8) 2764 (8K x 8)
RAM Upgrade	None	4164 (64K x 1)	4802 (2K x 8) 4804 (4K x 8)
KBytes per IN^2	1.19	1.45	1.33
Ultimate Matrix Capacity	16K x 8 EPROM 4K x 8 RAM	16K x 8 EPROM 64K x 8 RAM	> 64K x 8 Any Mixture

CONCLUSION

BYTEWYDE is a concept for the future which makes sense today. Alternative approaches have short comings which cause them to be less cost effective. Dynamic RAMs with x1 organizations are meaningful for large memory but inappropriate as a building block for smaller microprocessor memory. Static RAM like the 2114 1K x 4 require higher package count, offer no upgrade potential, and lack compatibility with ROM/EPROM. The printed circuit board density achievable with the BYTEWIDE concept is equivalent to the alternative approaches today and will be superior in the future without redesign. Memory cost is minimized by the increased engineering return on investment and economies to scale associated with prolonged usage of the same design.

DESIGN MEMORY BOARDS FOR RAM/ROM/EPROM INTERCHANGE

Application Note

Microcomputer-system designers can realize great benefits if their equipment has the flexibility of using mixtures of RAM, ROM and EPROM. For one thing, this capability allows them to take advantage of price differentials between memory-IC types; for another, it allows them to efficiently exploit these chips' different volatility characteristics.

This section details a method to achieve the desired flexibility: The technique it presents permits a single pc-board design to use multiple types of memory ICs. Furthermore, the method will work not only with today's devices, but with tomorrow's parts as well. Thus, you can use it to build systems that can readily be improved as technology advances.

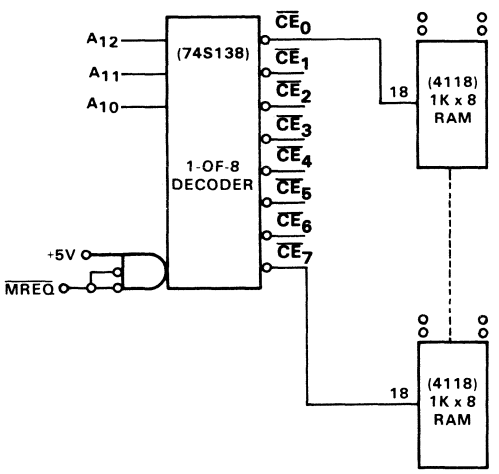
AIM FOR SOCKET COMPATIBILITY

At any time, the density of available single-chip ROM is as much as four times that of EPROM, while EPROM is as much as twice as dense as RAM. Because this approximate density relationship is expected to continue, a particular μ-C system design, if it is to have a long product life, must accomodate blocks of memory in as much as a 16:1 ratio. This requirement in turn dictates the need for a flexible address-space decoder: To accept devices that have an address space ranging from 1K to 8K, for example, a memory-IC socket must have a decoding mechanism that can accommodate such address-space differences.

A technique of programmable address-space management can meet this requirement. For memories of equal address space (same capacity), a simple 1-of-8 decoder such as the 74S138 works well (Figure 1). If you can limit memory usage to two different capacities, a 1-of-8 decoder, a quad AND gate and jumper wires (or a DIP switch) suffice (Figure 2). However, to support a wide range of memory capacities, a programmable bipolar ROM used as an address-space decoder provides the most flexible solution (Figure 3).

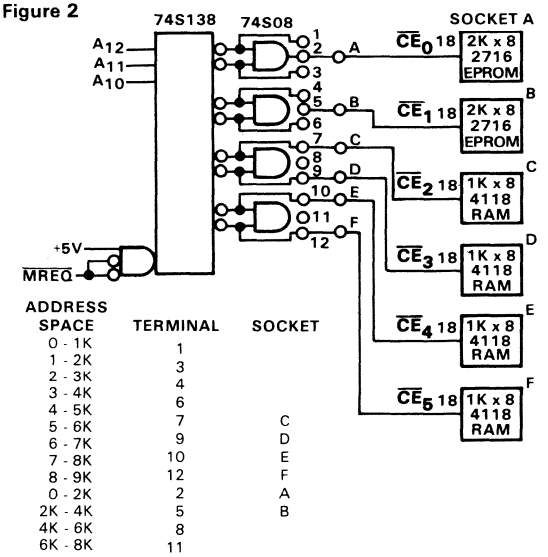
The most popular wide-word memory package today is the 24-pin DIP: It's used for the 4118 (1K x 8) RAM, the 2716 (2K x 8) EPROM, the 36000 (8K x 8) ROM, etc. But, although this 24-pin package serves today's devices, it can't support future higher capacity memory chips. The logical extension? A longer 28-pin package with the same center-to-center spacing and width. By using such a package and then carefully selecting their pinout

Figure 1



Address decoding for memories of identical capacity requires only a simple 1-of-8 decoder. A fixed 1K - word socket address space is shown.

Figure 2



A satisfactory address-decoding solution for memories with two different capacities employs a decoder, an AND gate and appropriate jumpers or switches. This technique handles 1K-or 2K-word devices equally well.

configurations, IC makers can obtain a high degree of compatibility between 24- and 28-pin memories—whether RAM, ROM or EPROM.

Fortunately for designers, such a trend is now very much in evidence. One example of such a 28-pin memory is Mostek's 4816 (2K x 8) RAM, soon to be joined by the 37000 (8K x 8) ROM and the 2764 (8K x 8) EPROM.

Note, however, that although the pinouts of various types of wide-word memories are similar, they are not exactly identical: Certain functions do not exist for all members of a manufacturer's family (WRITE ENABLE exists for the 4118 RAM, for example, but not for the 2716 EPROM). Additionally, multiple power supplies greatly complicate pinouts, so device compatibility is limited to parts that operate from +5V only.

Figure 4 takes all of these factors into account. It shows a layout of a 28-pin socket that maximizes the degree of device interchangeability among present and contemplated parts. Memory ICs with 24 pins plug into pins 3 through 26.

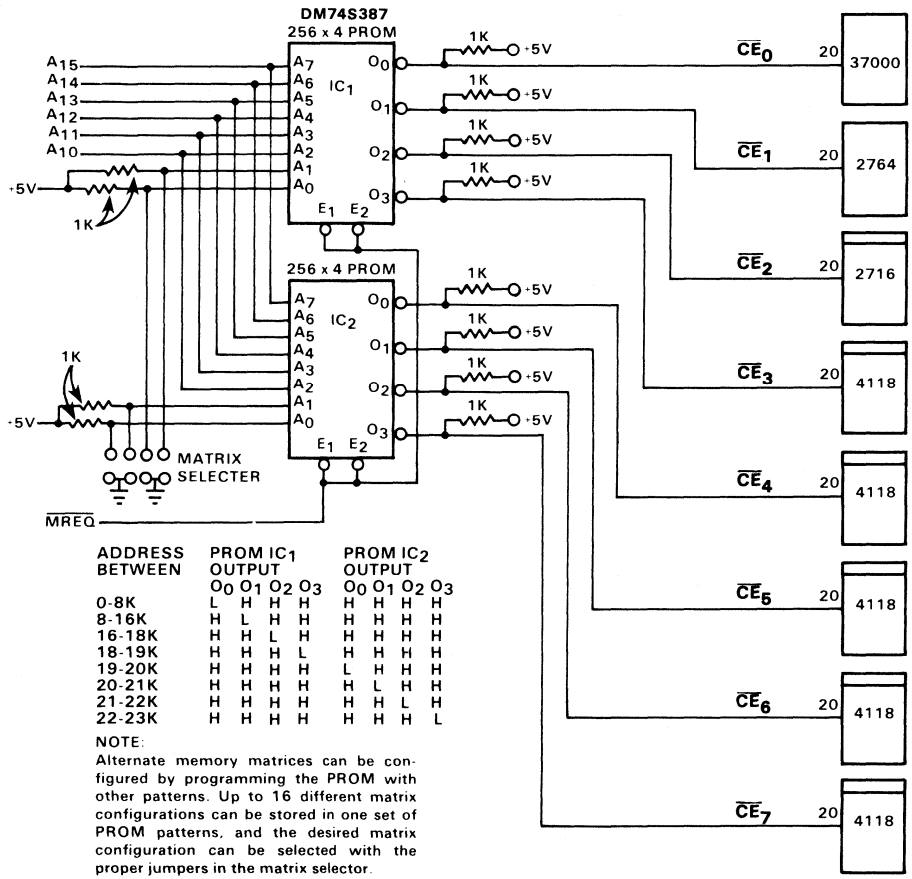
To put this pc-board design into perspective, consider Figure 5, which shows a 3880 μP interfaced to eight 28-pin memory sockets. By placing the proper pattern in the system's address-space PROM and selecting the appropriate jumpers, you can fill the memory sockets with any combination of today's (or tomorrow's) compatible RAM, ROM and EPROM devices.

INTERCHANGEABILITY PRODUCES MULTIPLE BENEFITS

The cost of any IC reflects its manufacturability and the volume in which it's produced.

Taking the latter factor first, increasing the volume of a

Figure 3



ADDRESS BETWEEN	PROM IC1 OUTPUT O_0 O_1 O_2 O_3	PROM IC2 OUTPUT O_0 O_1 O_2 O_3
0-8K	L H H H	H H H H
8-16K	H L H H	H H H H
16-18K	H H L H	H H H H
18-19K	H H H L	H H H H
19-20K	H H H H	L H H H
20-21K	H H H H	H L H H
21-22K	H H H H	H H L H
22-23K	H H H H	H H H L

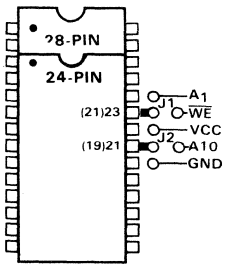
NOTE:
Alternate memory matrices can be configured by programming the PROM with other patterns. Up to 16 different matrix configurations can be stored in one set of PROM patterns, and the desired matrix configuration can be selected with the proper jumpers in the matrix selector.

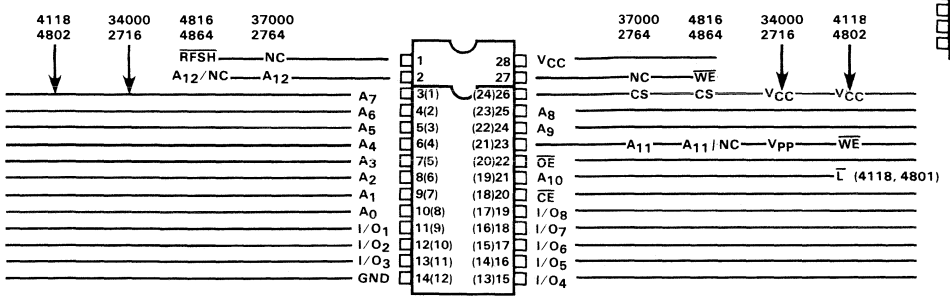
Programmable socket address space results from programming the PROM with a pattern corresponding to the desired socket address space. In this example, whenever an address between 0 and 8K is presented to IC_1, its O_0 output is LOW, and all others are HIGH.

Figure 4

COMPATIBILITY TABLE

MEMORY TYPE	PART NUMBER	CAPACITY	PACKAGE	JUMPER J1	JUMPER J2
ROM	MK34000	2K x 8	24 PIN	V_{CC}	A_{10}
ROM	MK37000	8K x 8	28 PIN	A_{11}	A_{10}
RAM	MK4118	1K x 8	24 PIN	$\overline{WE}$	V_{CC}
RAM	MK4802	2K x 8	24 PIN	$\overline{WE}$	A_{10}
RAM	MK4816	2K x 8	28 PIN	NC	A_{10}
RAM	MK4864	8K x 8	28 PIN	A_{11}	A_{10}
EPROM	MK2716	2K x 8	24 PIN	V_{CC}	A_{10}
EPROM	MK2764	8K x 8	28 PIN	A_{11}	A_{10}

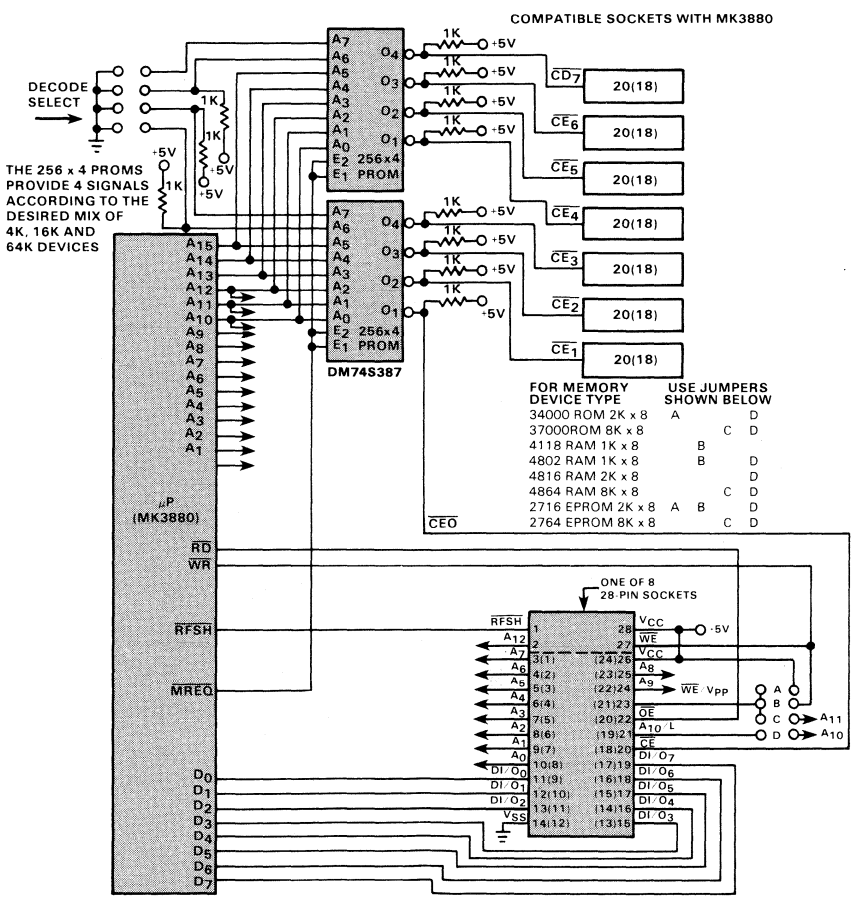




NOTE:
Parentheses indicate pin number of 24-pin packages
24-Pin devices are lower justified in pin 3 thru 26 of 28-pin socket

Key to the interchangeability concept is the use of a 28-pin socket to handle both 24- and 28-pin memory devices.

Figure 5



This μP-based system accomodates a wide variety of RAM, ROM and EPROM combinations through variations in the address-space PROM pattern and the jumper connections.

part substantially reduces its manufacturing cost. Thus, standard devices with widespread usage generally offer long-term price advantages. And because socket compatibility enhances a memory device's chances of achieving high-volume sales, it should provide users with substantial cost savings, while also increasing the likelihood of viable second sources.

Manufacturability of an IC relates to its die size and the number of steps in its manufacturing process. For a given defect density, the yield of good parts is geometrically proportional to size; ie, the smaller the chip, the greater its yield and the lower its cost. And of course, the fewer mask steps used to make the device, the lower the chip cost.

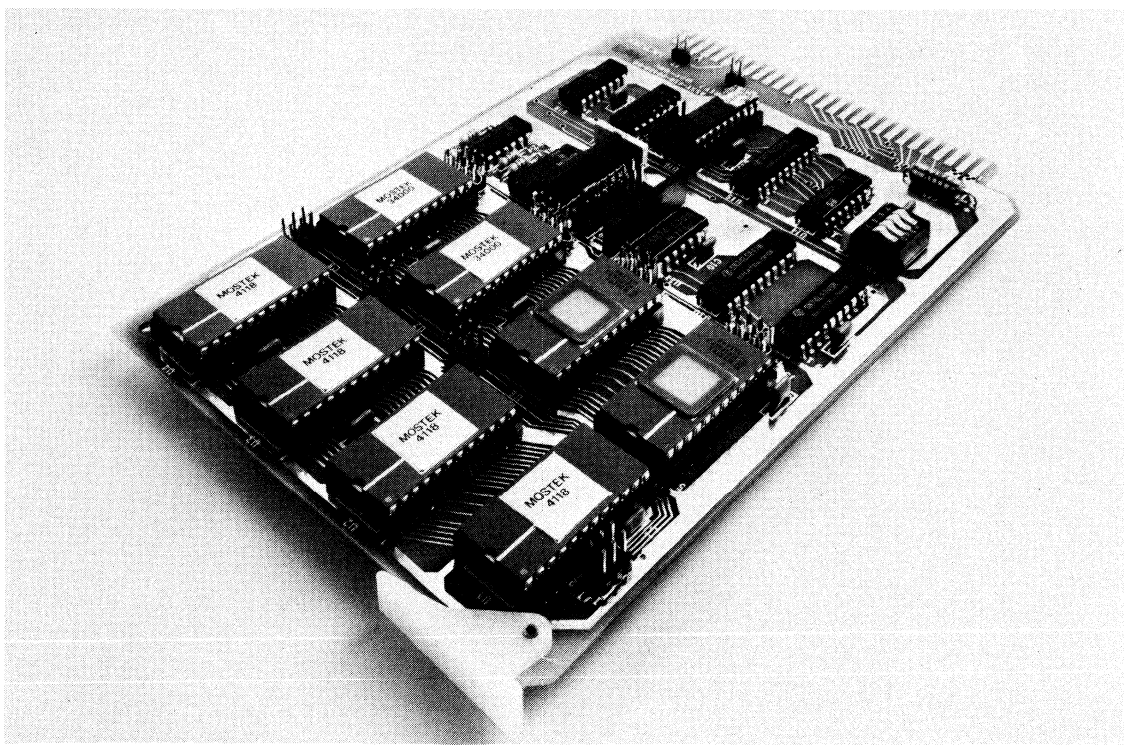
The accompanying table provides an understanding of the relative magnitudes of these factors.

	ROM (36000)	RAM (4118)	EPROM (2716)
Cell Size (mil²)	0.25	2.02	0.65
Number of Masks	8	11	13
Capacity (bits)	8K x 8	1K x 8	2K x 8

ONE BOARD DOES IT ALL

The viability and benefits of pin-compatible memory components are demonstrated by Mostek's Model MDX-UMC, a pc board that can handle 4118 (1K x 8) or 4802 (2K x 8) static RAMs, 2758 (1K x 8) or 2716 (2K x 8) EPROMs and the 34000 (2K x 8) ROM. This capability permits a total of 16 different memory configurations using 4K boundary addressing. Thus, MDX-UMC-based memories could include 4K x 8, 8K x 8 or 16K x 8 static-RAM boards; 4K x 8 or 8K x 8 ROM boards; or 8K x 8 EPROM boards.

MDX-UMC BOARD



MOSTEK®

NMOS RAM OFFERS NON-VOLATILITY WITH DATASAVE™

Application Note

INTRODUCTION

Non-volatile memory presents a paradox. On the one hand, data must be conveniently changed, while on the other hand, data must be safeguarded against loss. This problem can be likened to a door with a simple lock for normal entry, and a dead bolt latch for security. The non-volatile memory must have a simple method of purposeful change of data, yet have absolute protection against inadvertent loss of data.

At the system level storage requirements vary and not all memory need be non-volatile. In the past, memory was partitioned with regards to what must be retained and what could be lost. ROM and PROM were used for non-volatile storage, and RAM for volatile or temporary storage. The BYTEWYDE™ concept of RAM, ROM, and EPROM interchange has added flexibility to this type of memory design. The flexibility of memory interchange relieves many of the problems associated with predicting how much and what type of memory is needed. But there are many applications where interchange of memory is not enough. These designs are typified by the need to alter non-volatile memory.

Non-volatility is related to how difficult a device is to program or restrictions on the write cycle. ROM, for example, is factory programmable and is totally non-volatile. UV EPROMs can be altered in the field with some time and difficulty. UV EPROMs, and similar devices, have reduced non-volatility to a degree of inconvenience. The difficulty of altering the content of non-volatile memory has led to the development of new storage mechanisms for data retention. Many of the new storge mechanisms for memory are aimed at making the program cycle more closely emulate the read cycle. Ideally, a non-volatile memory should possess the following features:

1) Ease of use.
2) High density.
3) Write cycle performance equal to the read cycle.
4) Infinite number of program or write cycles.
5) High performance.
6) Low power and cost.

Many of the devices on the market have made progress towards meeting the list of requirements for a non-volatile memory. However, each technology explored to date falls somewhat short of what is required. For example, UV EPROMs need UV light for erasure and have a long program cycle. E^2PROMs, while being more convenient with electrical erasure, still have a long erase/program cycle and a limited number of write cycles. Shadow RAMs solve the write or program cycle problem, but have low densities because of the more complex cell.

A battery backup RAM can be a viable alternative to new technology methods of non-volatility if certain conditions exist. In order to be an effective solution, a battery backup RAM must use low power and be easy to implement. CMOS RAMs meet the low power requirement, however, the increase in processing needed for CMOS leads to higher cost. In fact, the most dense CMOS RAM available uses the same cell that has been used in Mostek static NMOS memory since 1977.

Proven NMOS memory technology combined with an innovative circuit design called DATASAVE is being introduced by Mostek. This 2K x 8 BYTEWYDE RAM, coupled with the advancements made in battery technology, bridges the gap between non-volatile memory and existing static RAM design (see Figure 1). The MK4802D-1 (DATASAVE) provides data retention using on chip circuits which switch to a standby battery when primary power failure occurs. A standby current of only 100μA is needed, since only the memory matrix and minimal support circuitry are maintained during the data retention mode. Low battery drain, ease of use, unlimited write cycles, read cycle equal to write cycle, and high performance make the MK4802D-1 an attractive offering.

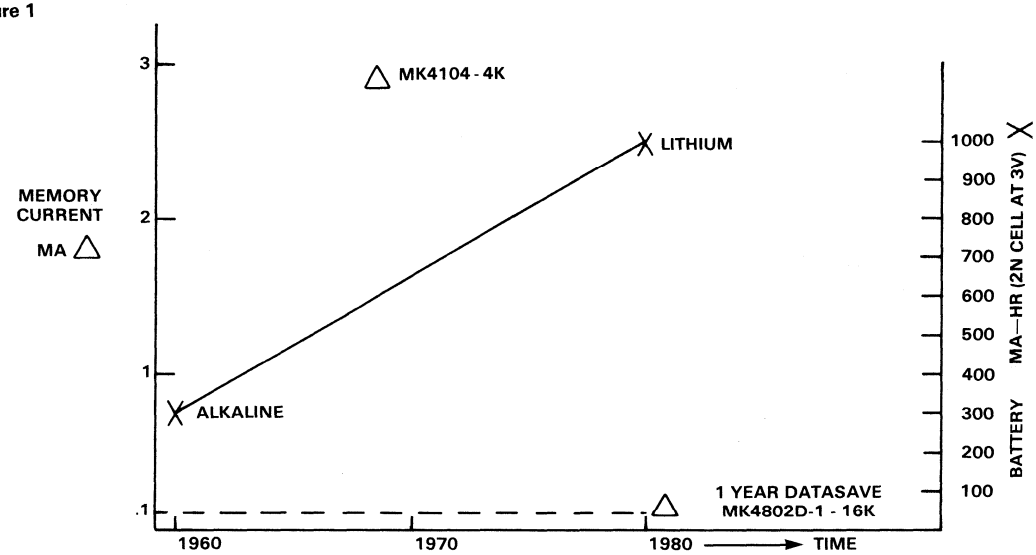
HOW IT WORKS

To accomplish the data retention mode, several new circuits and low power memory cells have been incorporated into the MK4802D-1. The new circuits consist of a voltage comparator which senses the status of V_{CC}, a switch to allow current to be sourced to the internal memory matrix from the $\overline{WE}$ pin instead of V_{CC}, and a standby charge pump needed to compensate for voltage changes, which are capacitively coupled to the substrate, when switching from DATASAVE.

The key to DATASAVE is the comparator and switch which put the memory in an ultra-low power write protected state (see Figure 2). The comparator monitors the status of V_{CC} and $\overline{WE}$. When $\overline{WE}$ is greater than V_{CC} by one volt ($\overline{WE} > V_{CC}$-1), the comparator output will activate a transistor switch connecting the $\overline{WE}$ pin to the memory matrix and inhibit all inputs/outputs. The memory matrix current will

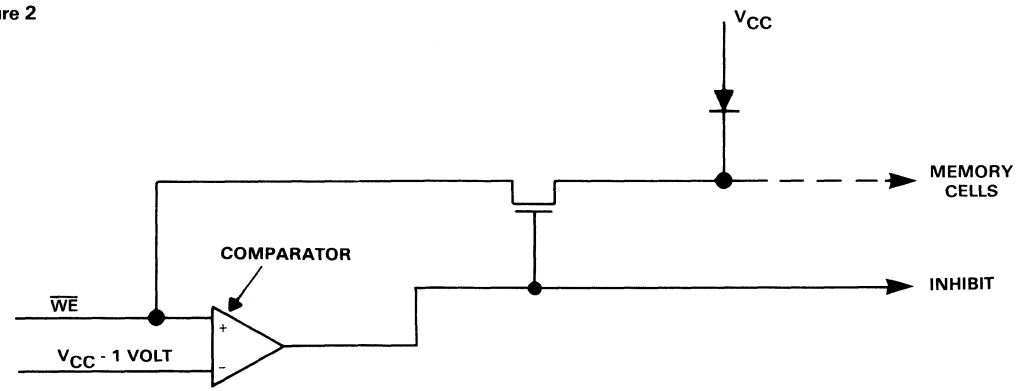
THE ECONOMICAL MK4802D-1 COMBINES WITH NEW BATTERY TECHNOLOGY OFFERING NON-VOLATILITY

Figure 1



MOSTEK'S DATASAVE™ ON CHIP FEATURE

Figure 2



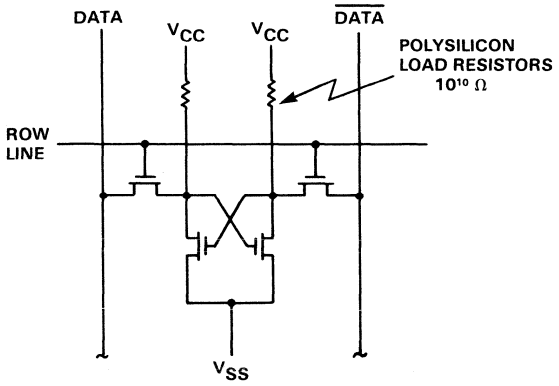
be sourced through the $\overline{WE}$ pin. All other circuits, with the exception of a standby charge pump and inhibit logic for the I/O, will become inactive as V_{CC} falls below write enable ($\overline{WE}$).

The standby charge pump provides bias which prevents the substrate from going positive during power up. This charge pump is a low power version of the larger charge pump which is active when V_{CC} is within specification.

The MK4802D-1 uses a low power cell consisting of intrinsic polysilicon resistors (see Figure 3) instead of the more power consuming depletion mode transistors. The low power is achieved because the resistor valve is of the order of 10^{10} ohms. Total matrix pull up current for thirty-two thousand resistors is approximately 30 μA. The resistors also help reduce cell size by permitting an efficient layout. Using Mostek's POLY 5 process, cell size is a mere 1.3^2mils.

LOW POWER CELL

Figure 3



SPECIFIC REQUIREMENTS

In order to successfully use DATASAVE, it is necessary to switch the $\overline{WE}$ pin from its normal function to the battery voltage prior to power failure. Battery supply to the $\overline{WE}$ pin during DATASAVE must be held between 4.0 Volts and 6.0 volts. External supply current to the memory is approximately 100μA during DATASAVE. Power supply slew rates need to be limited to 200μs/volt (see Figure 4).

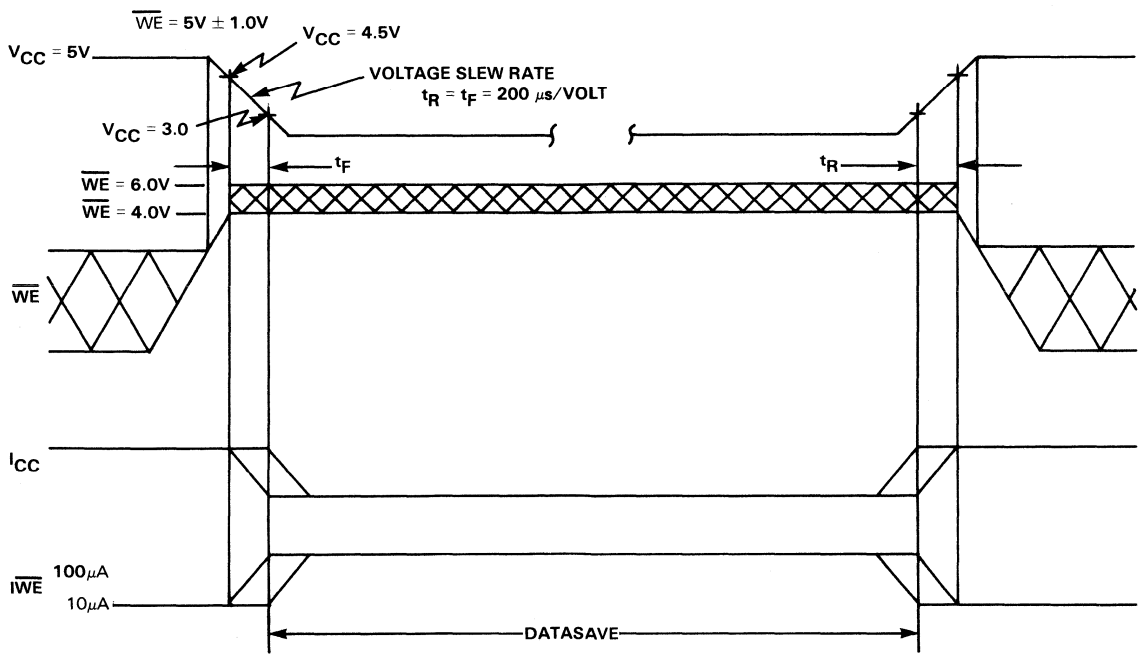
Power supply slew rate is a function of power supply design. The selection of the power supply used for V_{CC} in any battery backup design is an important matter. The power supply must have sufficient energy storage to hold V_{CC} within specification for some time after A.C. power is lost and meet the voltage slew rate specifications of the MK4802D-1 (see Figure 5). The proper selection of a power supply still does not solve the energy storage problem completely. Certain conditions, such as power supply malfunctions, blown fuses, etc., make it a wise precaution to have some additional storage capacity distributed throughout the system. Bypass capacitors provide some energy storage. However, the energy stored is far less than what is required. This can be illustrated by the following example. Assume a bypass capacitor size of .1MFD. Then C = I $\Delta t/\Delta V$ with ΔV = 1 volt and I = 125 MA (from the MK4802D-1 specifications) gives a slew time of .8μs. This exceeds the ΔV specified for the MK4802D-1. Energy storage must be supplemented with additional capacitance located at various points along the V_{CC} bus.

BATTERY BACKUP DESIGN

A sound battery backup design must be able to handle all types of power interruptions. Two power failure signals are required. One signal continuously defines the state of V_{CC}, while a second defines a change in the status of the power line.

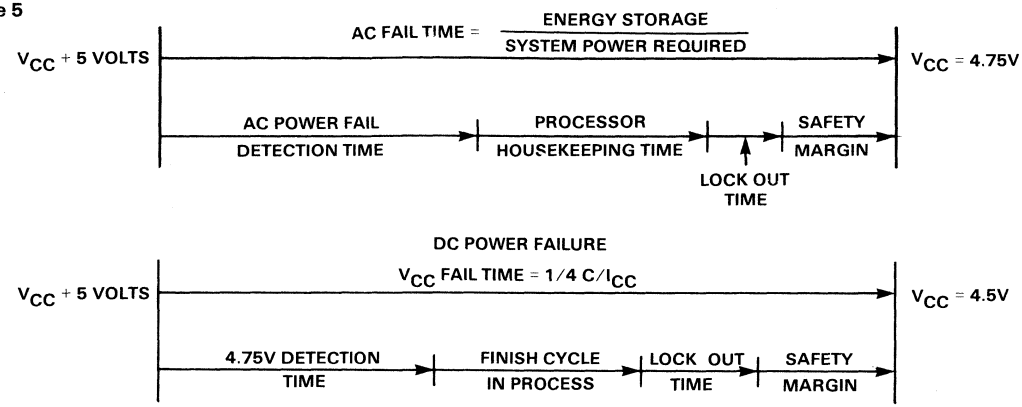
DATASAVE POWER SUPPLY REQUIREMENTS

Figure 4



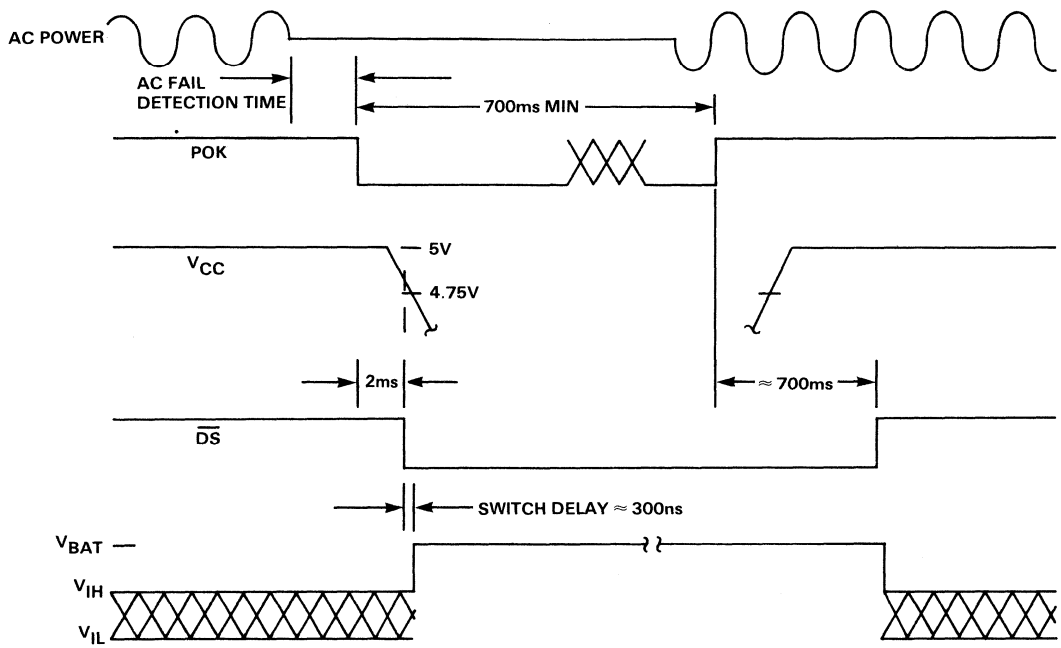
AC POWER FAILURES

Figure 5



AC POWER FAILURE SEQUENCE

Figure 6



In normal power outages (A.C. power loss), time for an orderly shutdown can be achieved if the power supply filter capacitor stores enough energy to hold V_{CC} within specification for several milliseconds after line power is lost. During this time the processor can execute last minute instructions prior to V_{CC} dropping below specification. After the necessary instructions have been executed, the processor may execute no-ops while $\overline{WE}$ is switched to the battery followed by V_{CC} going out of specification.

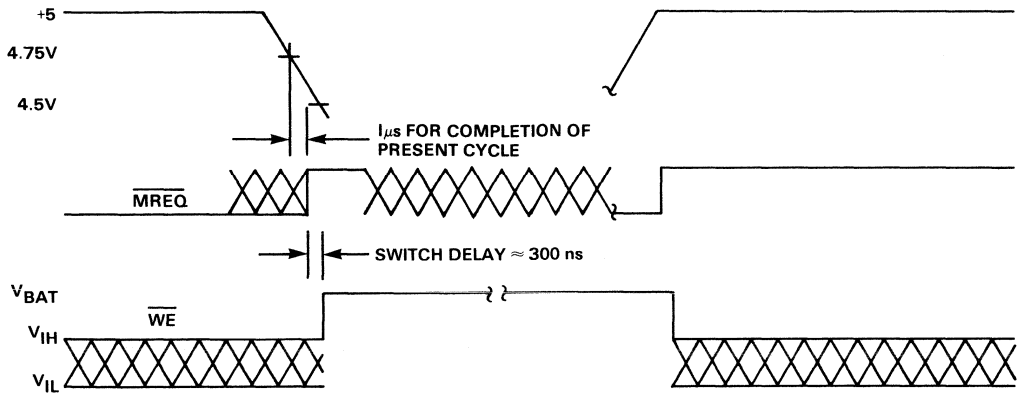
In abnormal power outages, such as D.C. failure or power brown outs, there may not be time for the processor to do any additional instructions. In these instances, the memory must be protected immediately after the completion of the present processor cycle. This type of power outage could occur in microseconds. Figure 6 illustrates the timing of a normal power fail sequence which results from A.C. power loss. Figure 7 illustrates D.C. power loss.

Some of the external sensing and switching circuits used in conjunction with DATASAVE must have a continuous power source. These circuits can be powered from the battery or be switched to battery prior to a power failure.

Battery choice is a function of application and selection

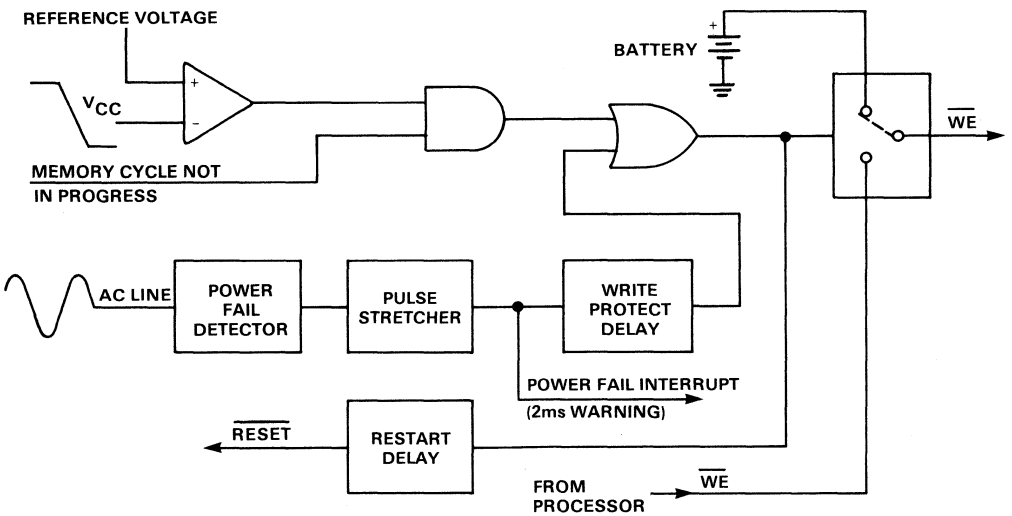
DC POWER FAILURE SEQUENCE

Figure 7



SYSTEM BLOCK DIAGRAM

Figure 8



should be based on performance and economy needed. A rechargeable battery should be used where power is constantly drained from the battery.

AN ACTUAL DESIGN

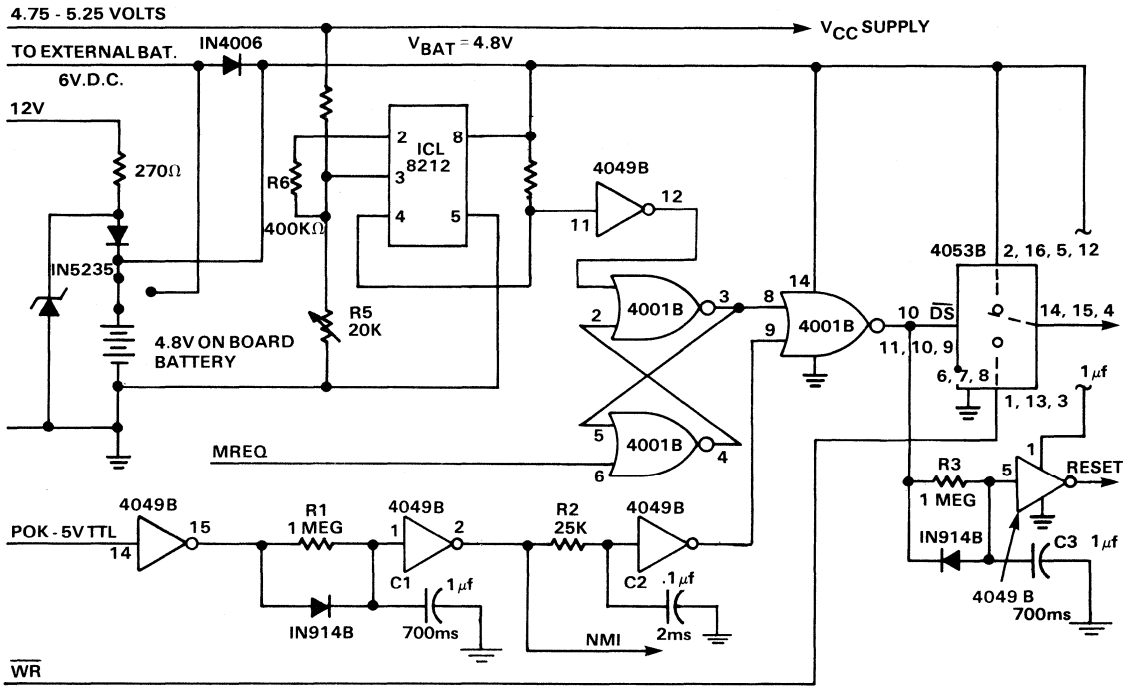
A circuit was designed to illustrate the usefulness of the DATASAVE feature in a system. The design requirements to be met in this application are as follows:

1) Sufficient battery to support 16K x 8 memory for 72 hours.
2) Foolproof power fail detection system.
3) Low battery drain current from the memory support circuitry.
4) Timing circuitry to allow for a microprocessor to do an orderly shutdown and automatic restart.
5) In-circuit battery charging.
6) Optional disposable batteries for economical designs.

In order to meet the above criteria, the logic of the system was designed to handle the two types of power interruptions (see Figure 8 for system block diagram). The normal shutdown is accomplished by sensing A.C. power line conditions. An A.C. line monitor must be used to convert the power line status to TTL levels. The A.C. power fail detector gives a low going TTL transition prior to V_{CC} going out of specification. This TTL signal, called Power OK or POK (see Figure 9), then creates a series of timed events. The first timing device provides a delay on the trailing edge

BATTERY BACK UP CIRCUIT USED TO IMPLEMENT DATASAVE

Figure 9



of POK. POK should be conditioned so that the system will not react to nuisance transients. Once POK goes low, future changes are inhibited for a time determined by R1C1. The timing tolerance should be long enough for the complete power fail sequence to time out. The second time delay (R2C2) has a more critical requirement to meet. Delay from this device allows time for the processor to do storage routines for an orderly shutdown. Time allotted by the R2C2 delay is dependent upon two factors. The first is the time needed by the processor to execute power down subroutines via the non-maskable interrupt as POK goes low. The second factor is the time the power supply can hold V_{CC} within specification after A.C. failure has occurred. The two restrictions on time need to be tailored to exact system needs. The 2MS of time, which is allotted in this design, is more than sufficient for the processor to do housekeeping. More time can be made available if the power supply used can hold V_{CC} in specification longer. In applications where the amount of time required is critical, more accurate timing elements and more energy storage can be used.

The output of the second time delay is one of two signals which can activate DATASAVE. A third time delay, R3C3, is required for automatic startup of the processor. R3C3 time needs to be long enough for V_{CC} to stabilize prior to turning control back to the processor since it restarts processor controlled memory cycles. For this design, an R3C3 time of 700MS was used.

The other method of detecting power failure is the D.C. monitor, which enhances the security of data. A combination comparator/reference is used to determine the status of V_{CC}. The output of the comparator is low when V_{CC} is valid. D.C. failure is detected when V_{CC} falls below 4.75V.

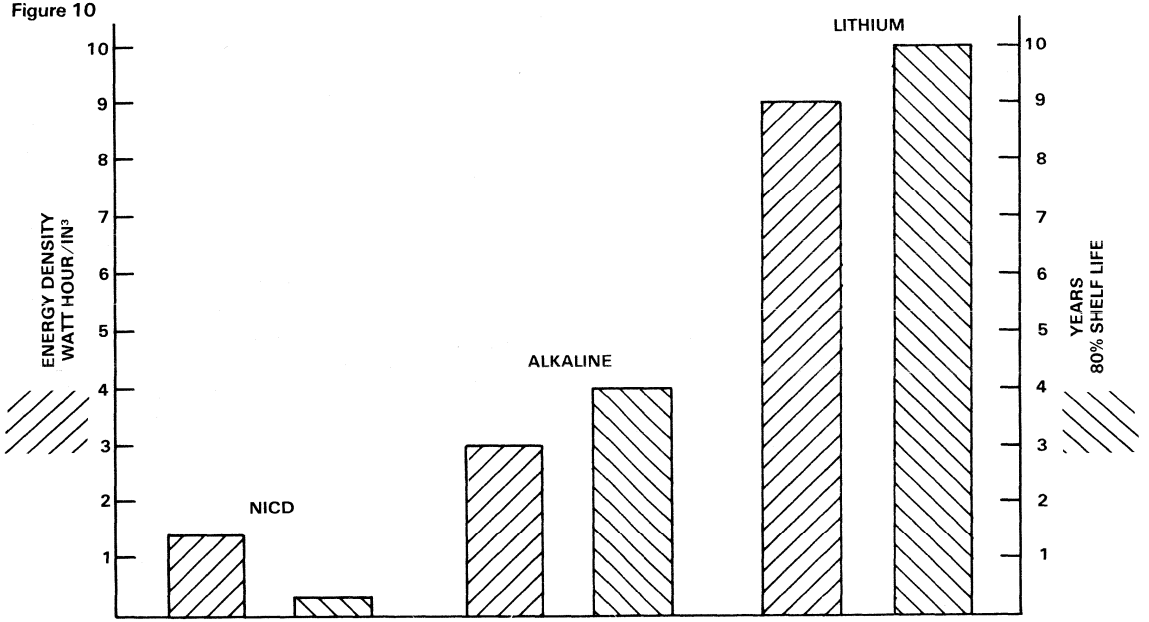
A reference is developed from an adjustable voltage divider (R4 and R5). The voltage divider is set so that 4.75 volts at V_{CC} provides the trip voltage of 1.15 volts. Resistor R6 provides for .25 volt of hysteresis and prevents undetermined outputs from the reference/comparator. The power fail condition readies a NOR flip-flop, which is activated by $\overline{MREQ}$ when the microprocessor goes to a memory inactive high state. When $\overline{MREQ}$ is high, the processor is not doing a memory cycle. The precaution of using $\overline{MREQ}$ to gate D.C. power fail prevents the $\overline{WE}$ line from being interrupted during a write cycle. Failure to take this precaution would mean that information could be lost.

D.C. power fail and POK are or'ed to produce the ($\overline{D.S.}$) DATASAVE signal which controls a CMOS switch. The CMOS switch will disconnect the $\overline{WE}$ pin from processor control and connect the battery supply in typically 300ns. The IR drop across the switch is .08 volt typical for a total memory standby current of 800μA.

The battery supply to support the DATASAVE circuit is

COMPARISON OF DIFFERENT N CELL BATTERY TECHNOLOGY

Figure 10



Technology	NI-CD	Alkaline MnO_2/ZN	Lithium MnO_2/LI
Application	Rechargeable	Non Rechargeable	Non Rechargeable
Cell Voltage	1.2 Volts	1.5 Volts	3 Volts
Size	2 x N Cell	2 x N Cell	2N Cell
MA - HRS	150	300	1000

flexible. If a chargeable battery supply is desired, a jumper-selectable charging circuit can be employed. Non-rechargeable batteries can also be used, and the charging circuit will supply power to the CMOS gates and V_{CC} detector while power is within specification. A blocking diode isolates the non-rechargeable battery during power up conditions. As D.C. power drops below the battery supply, current will start to flow from the battery. This type of arrangement prevents any battery discharge during normal power conditions, so that maximum battery utility is realized.

Battery technology affords a variety of options which can be put to use. High energy density is important for on board batteries. If a non-rechargeable battery is used, lithium batteries afford an inexpensive high energy density solution. Nickel cadmium is a good selection if a rechargeable cell is used. More complete protection can be obtained by a combination of rechargeable and non-rechargeable batteries. In such an arrangement, Ni Cd batteries could provide for short term power failures and long shelf life lithium batteries can provide an emergency reserve. Such an arrangement gives added security and protection through redundancy.

The selection of batteries is influenced by several factors. Shelf life, power density, mounting, rechargeability, and cost are important criteria.

Consistent packaging among various battery technologies helps in the selection process by giving the user an option if the requirements of the design changes. Several companies are presently involved in the manufacture of "N" size cell, which are available in Ni Cd, lithium, and alkaline (see Figure 10).

THE MK4802D-1 AT THE SYSTEM LEVEL

The advantage of a consistent packaging strategy for memories has been well-documented. Mostek's BYTEWYDE concept now takes on a new dimension with the MK4802D-1. This BYTEWYDE RAM with battery backup is interchangeable with all BYTEWYDE products. To illustrate this point, a complete memory board was designed with the following features:

1) Non-volatile memory using DATASAVE with all support circuitry included.
2) RAM, ROM, EPROM interchange.

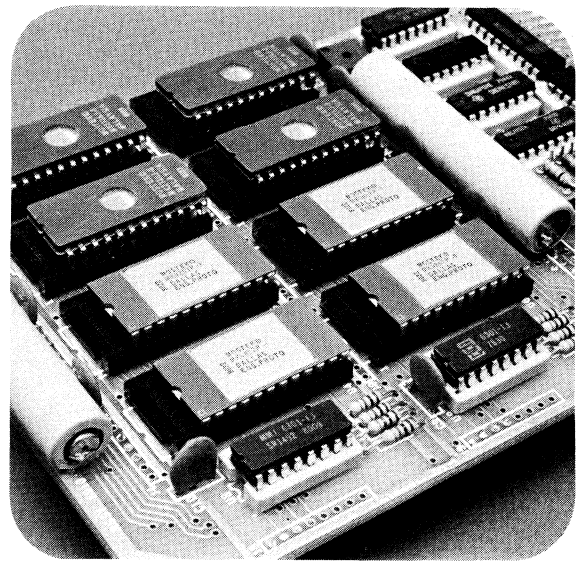
3) STD bus interface.
4) Expandable with technology advancements to 256K bytes of memory.
5) PROM address space decoding to facilitate different density levels of memory devices.
6) Provisions for both chargeable and non-rechargeable batteries.
7) 1000 hours of data retention, using lithium batteries at the 16K byte level of RAM.

This memory board was prototyped (see Figure 11) to test the BYTEWYDE design philosophy with DATASAVE concept. The schematic diagram (see Figure 12) shows ıe support logic discussed earlier. The eight 28 pin memory sockets could provide up to 256K bytes of memory capacity in the future.

CONCLUSION

The BYTEWYDE design philosophy combined with the MK4802D-1 DATASAVE RAM and current battery technology adds a new dimension to memory design. Low standby battery current and ease of use make the MK4802D-1 an attractive offering for those applications where non-volatile storage must be altered. The BYTEWYDE memory concept and DATASAVE help to bridge the gap between non-volatile devices and current RAM memories, while providing a better solution to a paradox.

BYTEWYDE MEMORIES WITH DATASAVE CIRCUITS AND STD BUS INTERFACE ON ONE BOARD
Figure 11

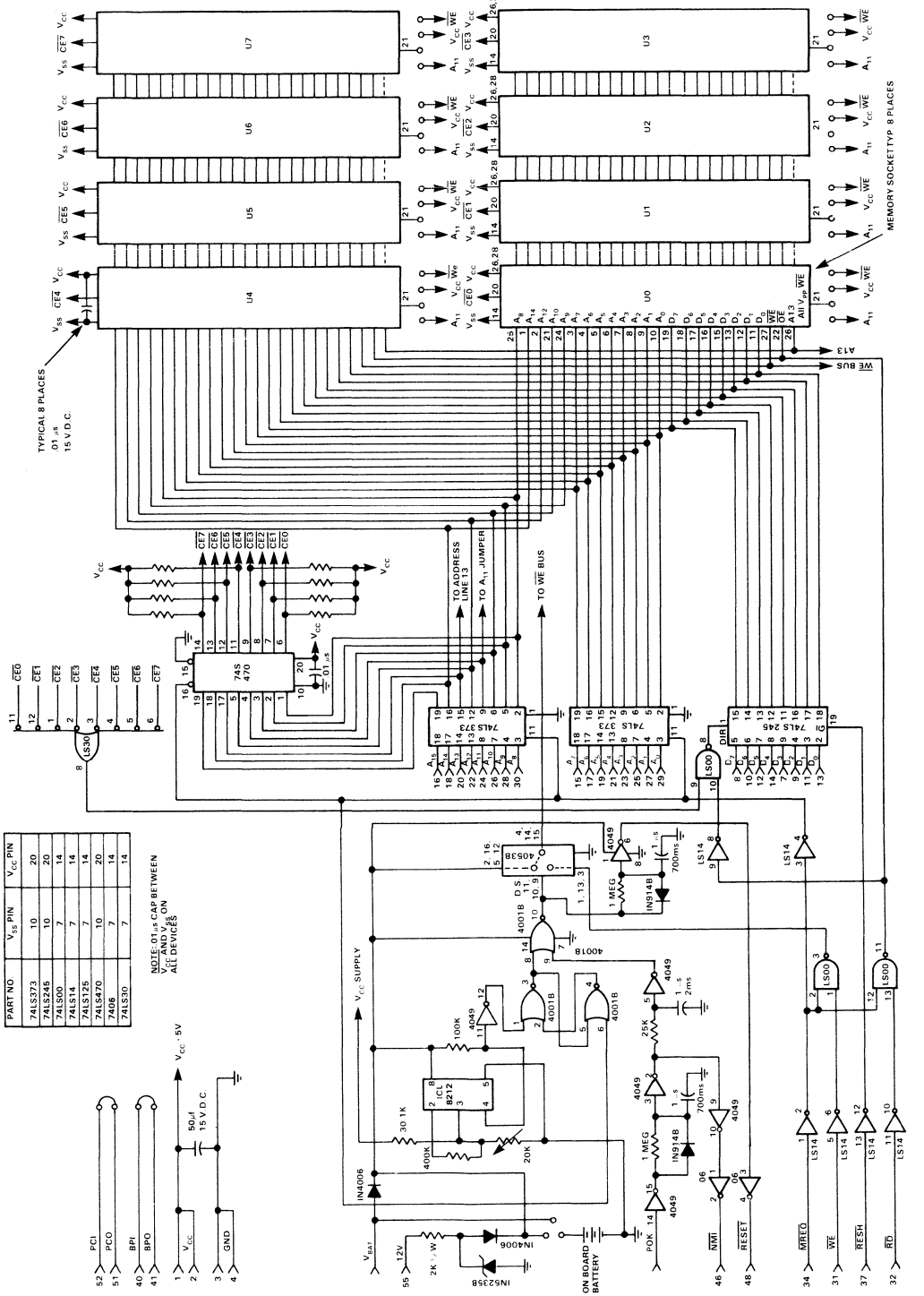


Acknowledgements:

W. J. Swain - Designer MK4802D-1
D. K. Lunecki - Product Engineer MK4802D-1

SCHEMATIC DIAGRAM OF THE BYTEWYDE MEMORY BOARD WITH DATASAVE AND STD BUS INTERFACE

Figure 12



MOSTEK®

MK4801A/MK4802 FOR HIGH SPEED APPLICATIONS

Application Note

Designers of high speed memory systems have a new option when it comes to selecting the configuration of their memory array. As N-channel MOS technology follows its customarily aggressive development patterns, two new parts, the 1K x 8 MK4801A and the 2K x 8 MK4802 are becoming available offering density, configuration advantages, and ease of use features not available on 4K density devices. These parts are pin compatible static RAMs utilizing Mostek's POLY 5™ scaled NMOS process. This process combines the density improvement which keeps the die size small for aggressive pricing with the short channel lengths required to place a part in the high speed race.

The relationship between the parts extends beyond similar pinouts and part numbers. The pictures in Figure 1 show the die for both parts and reflect the fact that the MK4802 has a heritage which traces directly to the MK4801A. So the peripheral circuitry and the cell used in both parts are basically the same, with the MK4801A having more maturity while the MK4802 has some design advantages aimed at making the part more versatile.

WHY BYTEWYDE?

Organizing memory chips so that a single IC can interface to a bidirectional data bus is not a new idea; it goes back to small PROMs and to the 6810 256 x 8 static RAM. However, the high density RAM market had effectively ignored the 24 pin by 8 pinout made so popular by EPROMs until the MK4118 was introduced in 1978. This microprocessor-oriented 1K x 8 static RAM is being joined in the market place not only by Mostek's two new static RAMs, but also by a host of other manufacturer's 2K x 8 static RAMs. This flurry of activity validates that the BYTEWYDE™ approach has advantages in certain segments of the market.

The BYTEWYDE concept of memory compatability has taken this base 24 pin package and developed it into a socket compatible family of RAM, ROM, and EPROM. JEDEC has accepted the 28 pin level of density and has used it for the basis of a new memory standard for by 8 parts. Up to now, BYTEWYDE parts like the MK4118 1K x 8 static RAM have served as building blocks with moderate performance aimed at the microprocessor designs. However, many of these benefits carry over to the sub-100ns market.

Fast RAM applications are often in wide word configurations. Video buffers, cache memories, and writable control stores have typical arrangements of 2K x 8, 4K x 32 and 4K x 64, respectively. The benefits of BYTEWYDE which apply to the users are the layout advantage, incremental expansion, density, upward compatability, and the presense of an extra control function.

"FORM FACTORS" OF BY 8 MEMORIES

Advantages of the pinout used in the MK4801A/MK4802 start with the simple fact that these parts are both specification and pin compatible. Once the socket is laid out, the parts are completely interchangeable. This upward compatability is built into the BYTEWYDE pinout. The 28 pin package has sufficient capacity to handle 15 address lines and can accomodate 32K bytes of memory, once the technology can put that on a piece of silicon. Figure 2 shows how the MK4801A/MK4802 fit into this family of parts.

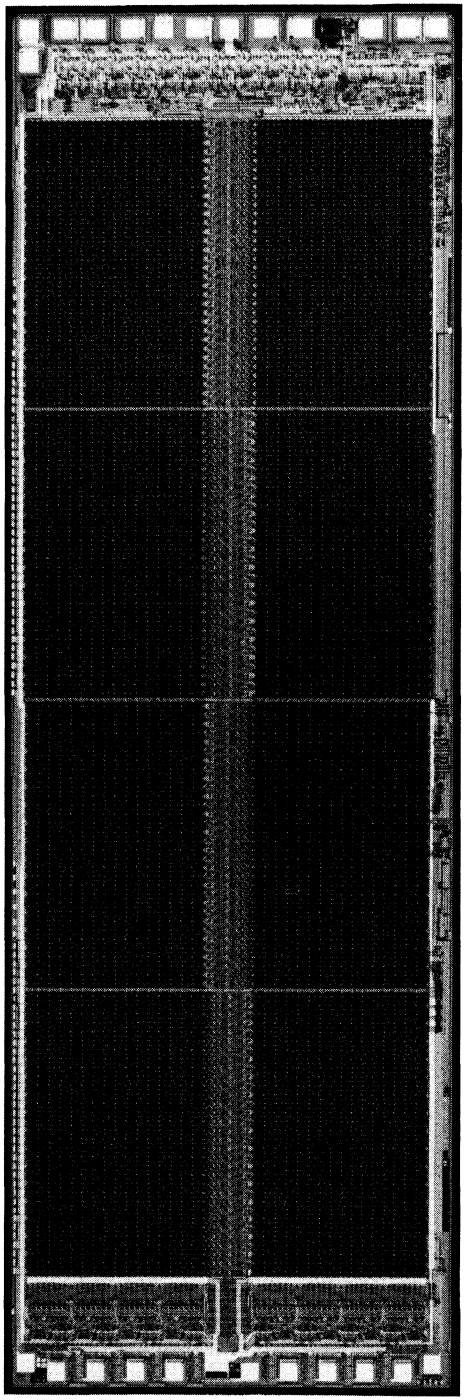
Using a by 8 internal structure has definite advantages for many users from a printed circuit density standpoint, compared to by 1 static memories for applications which require a minimal memory depth relative to word width. For instance, a system requirement needing 8K x 8 of RAM will not be able to take advantage of new generation 16K x 1 products without wasting half of the capacity (the upper 8K). Using BYTEWYDE memories results in better matching of the memory to the actual system configuration.

A side issue of the above argument is that of incremental modular expansion. If a user has by 1 parts in his system and exceeds the capacity of the memory allocated to him by the hardware designer, memory expansion will not come cheap. To go in any additional depth, 8 chips must be added, tacking on another 4K bytes when maybe only 1K bytes were required. Also, since memory expansion represents a considerable hardware modification, the extra chip locations are layed out in anticipation of adding the extra memory chips later. Then if there is no expansion requirement, P.C. real estate was wasted.

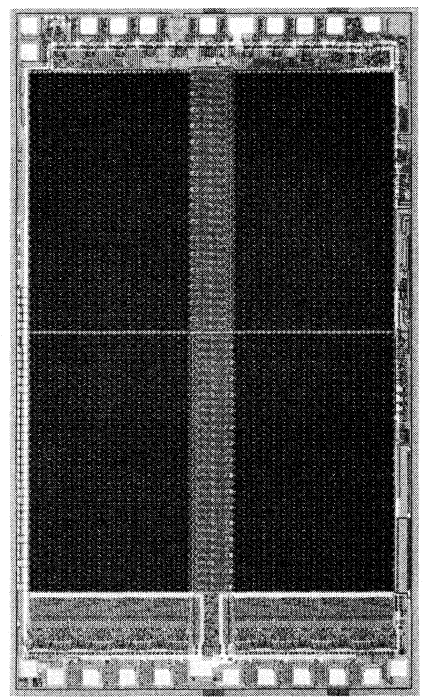
When a designer chooses BYTEWYDE, he can expand the system in 1K byte increments, avoiding manufacturing products that waste P.C. real estate. Also, just as the 2K x 8 MK4802 can replace the 1K x 8 MK4801A, this pinout offers the user the flexability of memory expansion via new higher density 28 pin memory product introduction.

DIE PHOTOGRAPHS

Figure 1



MK4802
Dimensions - 331 mil. x 108 mil.
Area - 35748 sq. mil.



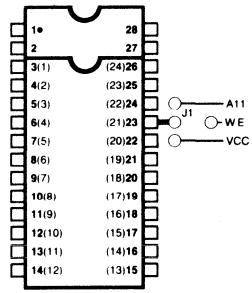
MK4801A
Dimensions - 106mil. x 182 mil.
Area - 19292 sq. mil.

BYTEWYDE TABLE

Figure 2

Memory Type	Part Number	Capacity	Package	Jumper J1
ROM	MK34000	2K x 8	24 Pin	NC
ROM	MK37000	8K x 8	28 Pin	A11
ROM		32K x 8 △	28 Pin	A11
RAM	MK4802	2K x 8	24 Pin	WE
RAM		4K x 8 △	28 Pin	A11
RAM	MK4118A/4801A	1K x 8	24 Pin	WE
EPROM	MK2716	2K x 8	24 Pin	VCC
EPROM	MK2764 △	8K x 8	28 Pin	A11

△ available 1981



4118/A 4801A	4802	34000	2716	4K x 8	37000	32K x 8	2764		2764	32K x 8	37000	4K x 8	2716	34000	4802	4118A 4801A
				NC	NC	A14	NC	1 28	VCC	VCC	VCC	VCC				
				NC	A12	A12	A12	2 27	NC	NC	NC	$\overline{WE}$				
A7	A7	A7	A7	A7	A7	A7	A7	3(1) (24)26	NC	A13	NC	NC	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6	A6	4(2) (23)25	A8	A8	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	A5	A5	5(3) (22)24	A9	A9	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	A4	A4	6(4) (21)23	A11	A11	A11	A11	VPP	NC	$\overline{WE}$	$\overline{WE}$
A3	A3	A3	A3	A3	A3	A3	A3	7(5) (20)22	O E VPP	O E	O E	O E	O E	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2	A2	A2	A2	8(6) (19)21	A10	A/O	A10	A/O	A10	A10	A10	NC
A1	A1	A1	A1	A1	A1	A1	A1	9(7) (18)20	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0	A0	A0	A0	10(8) (17)19	D7	D7	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	D0	D0	D0	11(9) (16)18	D6	D6	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	D1	D1	D1	12(10) (15)17	D5	D5	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	D2	D2	D2	13(11) (14)16	D4	D4	D4	D4	D4	D4	D4	D4
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	14(12) (13)15	D3	D3	D3	D3	D3	D3	D3	D3

Parenthesis Indicates Pin Number of 24 Pin Packages.
24 Pin Devices are Lower Justified in Pins 3 Thru 26 of 28 Pin Socket

EXTRA CONTROL

When by 1 memories are used, a single control function (chip enable), is sufficient to allow complete control over the chip's output buffers. This is because most by 1 memories have separate I/O with DATA IN and DATA OUT that are run through separate buffers whose enable controls for interfacing to common I/O busses are provided via the control functions on external bus buffers. When a bi-directional data bus is used, the need becomes much more important for an output enable ($\overline{OE}$) control function to control the time multiplexing of DATA IN and DATA OUT.

Bus contention can result without proper use of the $\overline{OE}$ control when memories are pushed to their full performance. There are ways in which interfaces between memories and their drivers can leave potential overlap in the control of the data bus. One of the most common examples of a need for independent control of the outputs when using such a fast part is during the write cycle. As shown in Figure 3, the $\overline{WE}$ control needs to be brought high t_{WPL} before the cycle actually ends. This time, equal to 50ns in the -70 parts, allows internal completion of the write cycle. After this time has elapsed, a read cycle will begin which may not be apparant to the outside world. If $\overline{CE}$ is held low for too long, a read access will occur and the memory's outputs will turn on. Since this is occurring amidst a write cycle, the opportunity exists for the memory's and the data buffer's outputs to be in contention. With an $\overline{OE}$ control this can be avoided.

Proper system design should be able to get around this type problem, but that 50ns t_{WPL} is a maximum over the temperature range with no minimum specified. Bus contention can be something which is a function of particular ICs interacting together, and is very difficult to analyze. Also, when these output buffers begin to fight they tend to bother neighboring circuitry. Current peaks the order of 400ma due to short circuits tend to couple to other traces and if a false signal coupled to something like the $\overline{CE}$ lines, a difficult soft error debug problem lies ahead.

High speed memory design relies on predictable performance and since minimum access times are not specified, having $\overline{OE}$ control capability is necessary for a worst case design to provide for trouble-free system manufacturing.

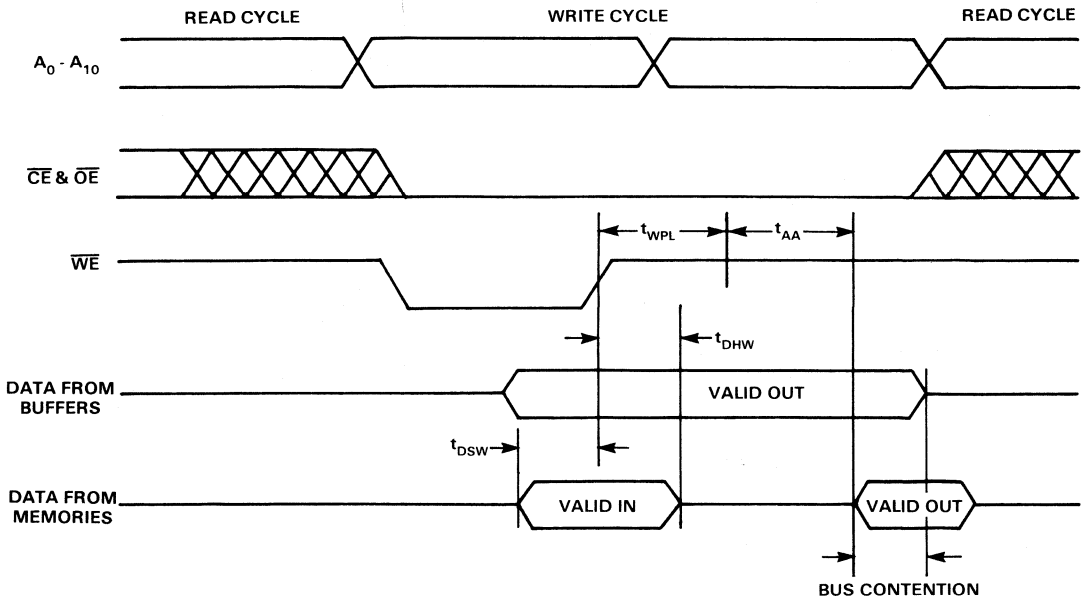
LAYOUT

Packaging considerations play a large role in the selection of the type of memory used in an individual application. Currently, there are three configurations in which sub-100 nanosecond RAMs are readily available. Figure 4 shows the MK4801A/MK4802 in the 600mil package with the two 300mil alternatives, the 4K x 1 2147 and the 1K x 4 2148.

Applications for these devices fall into three categories, those favoring by 1 organization, those favoring wide word organization, and those which lie between the extremes.

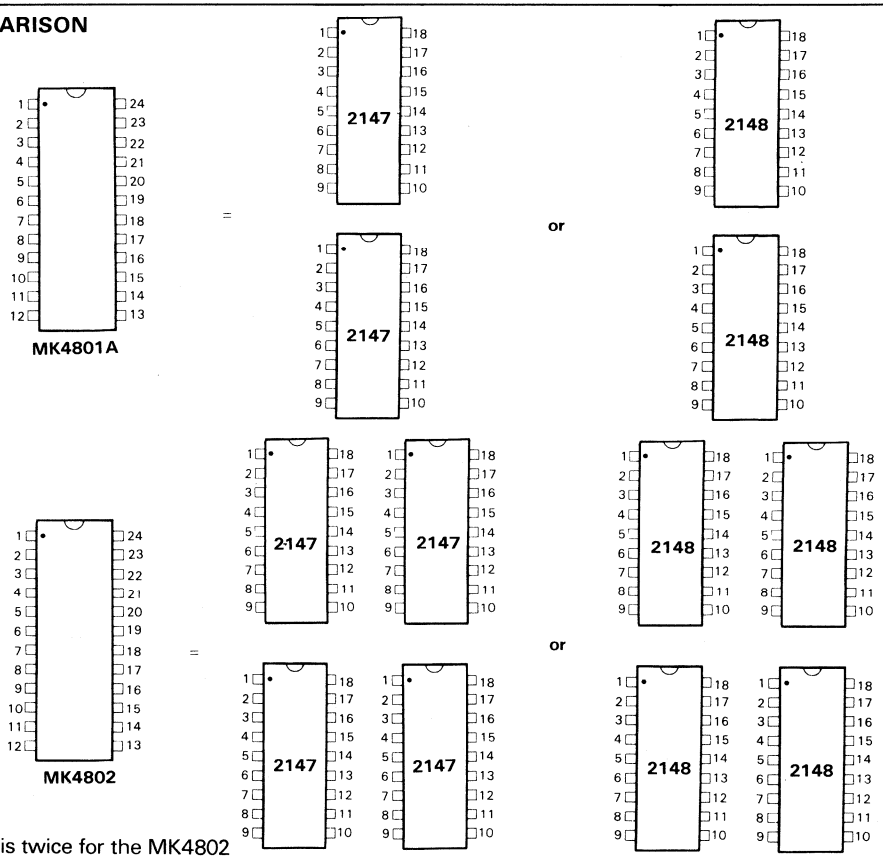
BUS CONTENTION WITHOUT PROPER USE OF $\overline{OE}$

Figure 3



DENSITY COMPARISON

Figure 4



P.C. Board density is twice for the MK4802

When a memory array's organization is shallow but wide, the wide word devices have layout advantages over the by 1 devices. Consider an application which could accept either memory type. The designer of a high speed 4K x 32 buffer memory can use 32 4K x 1 memories, or 16 1K x 8 devices. If the 2147 type by 1 is selected, then a layout difficulty will result. The designer could run a string of 32 devices in a row, matching the 4K x 32 nature of the array, but that will result in an overdrive condition for a single address buffer. Since square arrays provide better packaging and give short P.C. traces, the designer will probably lay the array out as shown in Figure 5, with 4 rows of 8 devices each. Compare this to the way in which the by 8 MK4801A will pack in a 4 by 4 array. A number of layout advantages exist for the by 8 array. The simple fact that there are half the chips cuts down the number of required address and control drivers. If the board is designed with rules requiring 1 driver per 8 inputs, the by 1 array will need 4 sets of 14 drivers, twice the number needed in the by 8 arrays. Also, the by 8 array takes better advantage of the data buffers with 4 memories per driver versus 1 memory per driver in the by 1 array.

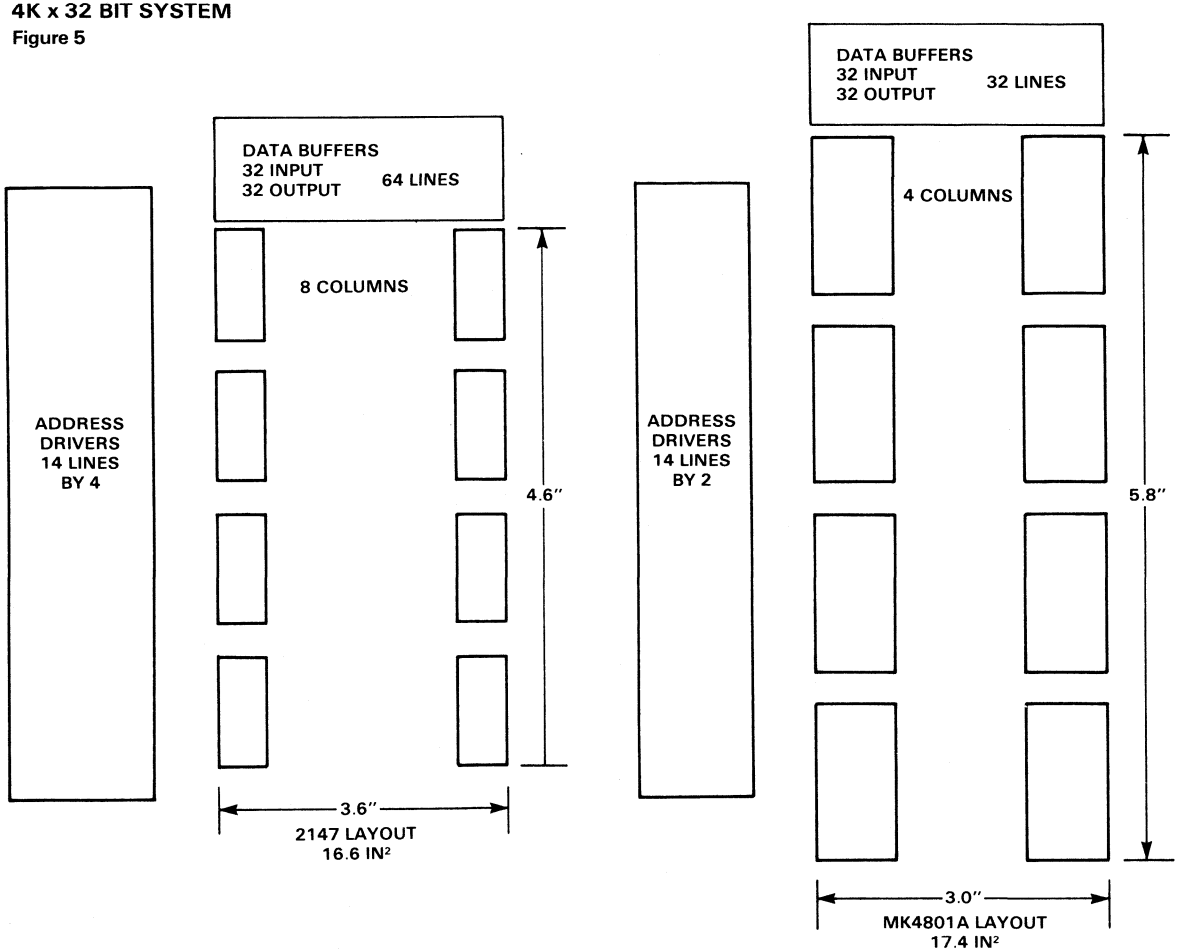
Limitations with the amount of room for P.C. traces also enter into the picture. With a single column of the by 1 array, 4 DATA IN and 4 DATA OUT lines must be run to the data I/O buffers, which are just too many to fit into the space provided. Therefore, in a realistic system, either more space must be provided, or a multi-layer card must be used for the by 1 type devices.

So where does the 2148 type device fit into this picture? As a wide word device (1K x 4) any argument which applies to a by 4 device also applies to a by 8 device. However, with equivalent packing densities in the 2148 versus the MK4801A, the by 8 devices carry the wide word advantage to the byte level. This has advantages as densities increase. If the preceding comparison looked at the 16K MK4802, the packing density would be twice that of the 18 pin devices.

DEVICE OPERATION

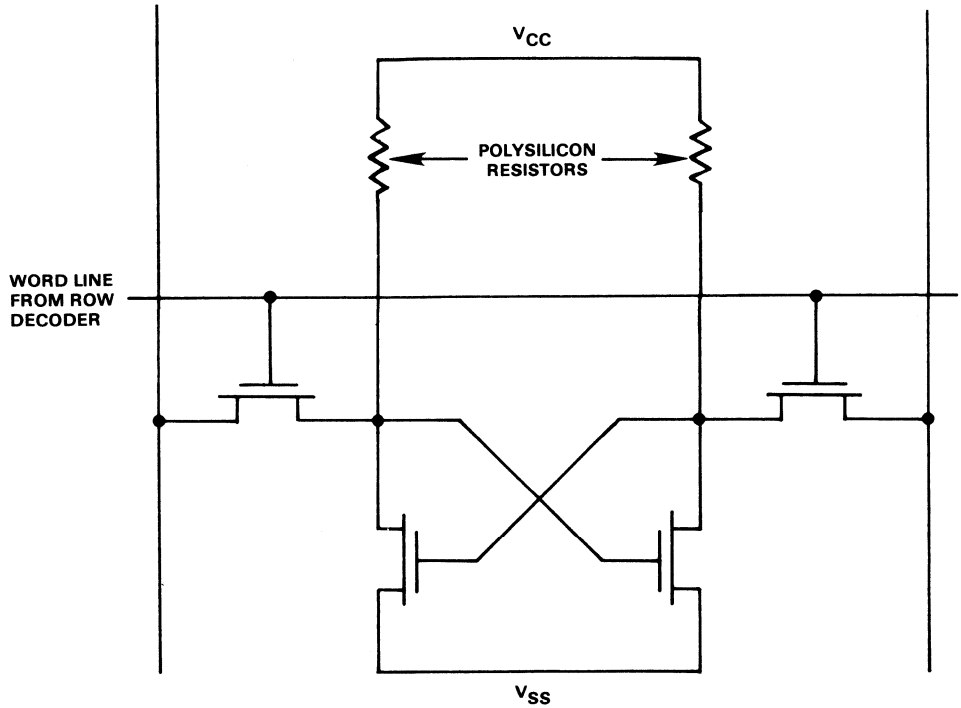
Mostek's static RAMs combine the external characteristics of purely static operation with the advantages of internal

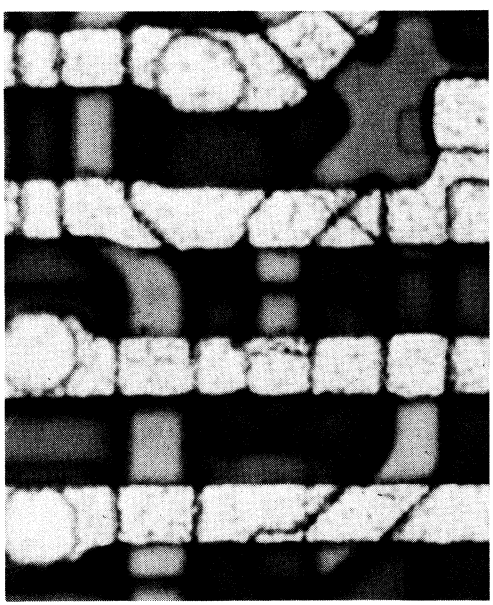
COMPARING BY 1 TO BY 8 DEVICES
4K x 32 BIT SYSTEM
Figure 5



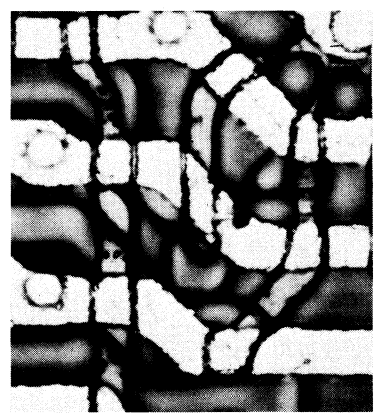
POLYSILICON STATIC RAM CELLS

Figure 6





MK4104 1976
2.75 mil²



MK4801A/MK4802 1980
1.3 mil²

dynamic periphery on the chip. The static cell used in the MK4801A/MK4802 is becoming a standard in the industry, following its introduction in the 4K x 1 MK4104 back in 1976. By employing polysilicon resistors instead of depletion load transistors, the MK4104 achieved a drastic reduction in cell size and cell power dissipation. Dimensional scaling along with processing and layout improvements have allowed the static cell to be reduced to 1.3 square mils. Figure 6 shows the comparison between cells, along with the cell's schematic diagram.

The peripheral circuitry surrounding the memory matrix is where the dynamic nature of the chip enters in. Clocked sense amps and clocked decoder circuits provide fast N-channel MOS performance without consuming large amounts of steady state power. Figure 7 shows an oscilliscope photo of the current consumption in a MK4801A. Here, peak currents of 136ma were measured during the cycle, with the DC paths in the part only consuming 36ma. The resulting average I_{CC} current is much less than the data sheet specification of 125ma, however lower temperature operation and processing variations will affect the "typical" average I_{CC} consumption as the process is optimized for speed.

Read and write cycles operate under different system considerations, and Mostek has developed these memories to recognize this fact. The result is a ripple through read, and an Edge Activated™ write cycle.

ADDRESS ACTIVATED™ READ

Read cycles operate in a completely static mode; they require no external clocks for proper operation. A true ripple through operation results from an address change. The photo in Figure 7 shows changes in DATA OUT in response to an address change only; the control signals remained low. Referring to the internal logic diagram of Figure 8, all address lines feed into buffers which generate a SAT pulse. It is the trailing edge of this pulse which initiates the Ø1 clock shown in the figure. This pulse, for Sense Address Transition, is generated whenever any of the address lines change logical states. It is the SAT detectors which allow these RAMs to appear completely static in the read mode.

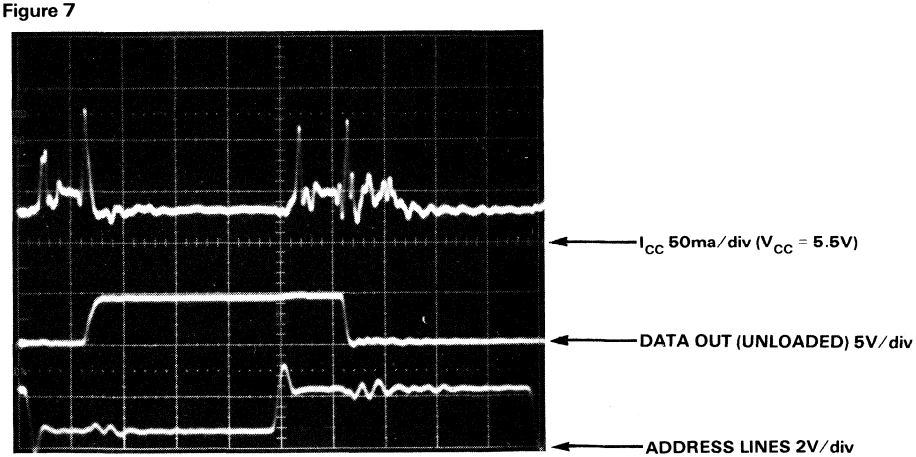
These timing diagrams show two different types of access times. The t_{AA} shown in the timing diagram of Figure 9 reflects the full rated speed of the part. This means that the fastest access is initiated upon address transitions and is measured from the time at which the last address line is stable. The other two times, t_{CEA} and t_{OEA}, are equal to half of t_{AA}. Referring to the logic diagram of Figure 8, it can be seen that when $\overline{WE}$ is high, the only effect that $\overline{CE}$ and $\overline{OE}$ have is upon the buffer and in the read mode this is the only function for both the $\overline{CE}$ and the $\overline{OE}$ controls.

Data appears at the output via a rather straightforward procedure. There are eight arrays of 128 x 8 cells each representing one of the eight parallel outputs. Seven of the address lines feed into a row decoder which selects one of 128 rows (for the MK4802, there are 256 rows, one of which is selected by 8 of the address lines). Then all eight cells in each row dump their data onto the metal data and $\overline{data}$ lines running the length of the array. The three remaining address lines feed into a column decoder which then select one of eight sense amps at the top of each memory matrix. It is the fact that the data and $\overline{data}$ lines are low resistance metal which allows the MK4801A to be doubled to produce the MK4802 while keeping the same data sheet specs. Propagation delays along these metal lines (which are double in length) are short compared to the more resistive polysilicon row lines (which keep the same length) which feed the outputs of the row decoder into the array.

On the trailing edge of the Ø1 clock, the selected sense amp will provide drive to the output buffer. Assuming that $\overline{CE}$ and

CURRENT CONSUMPTION PER CYCLE

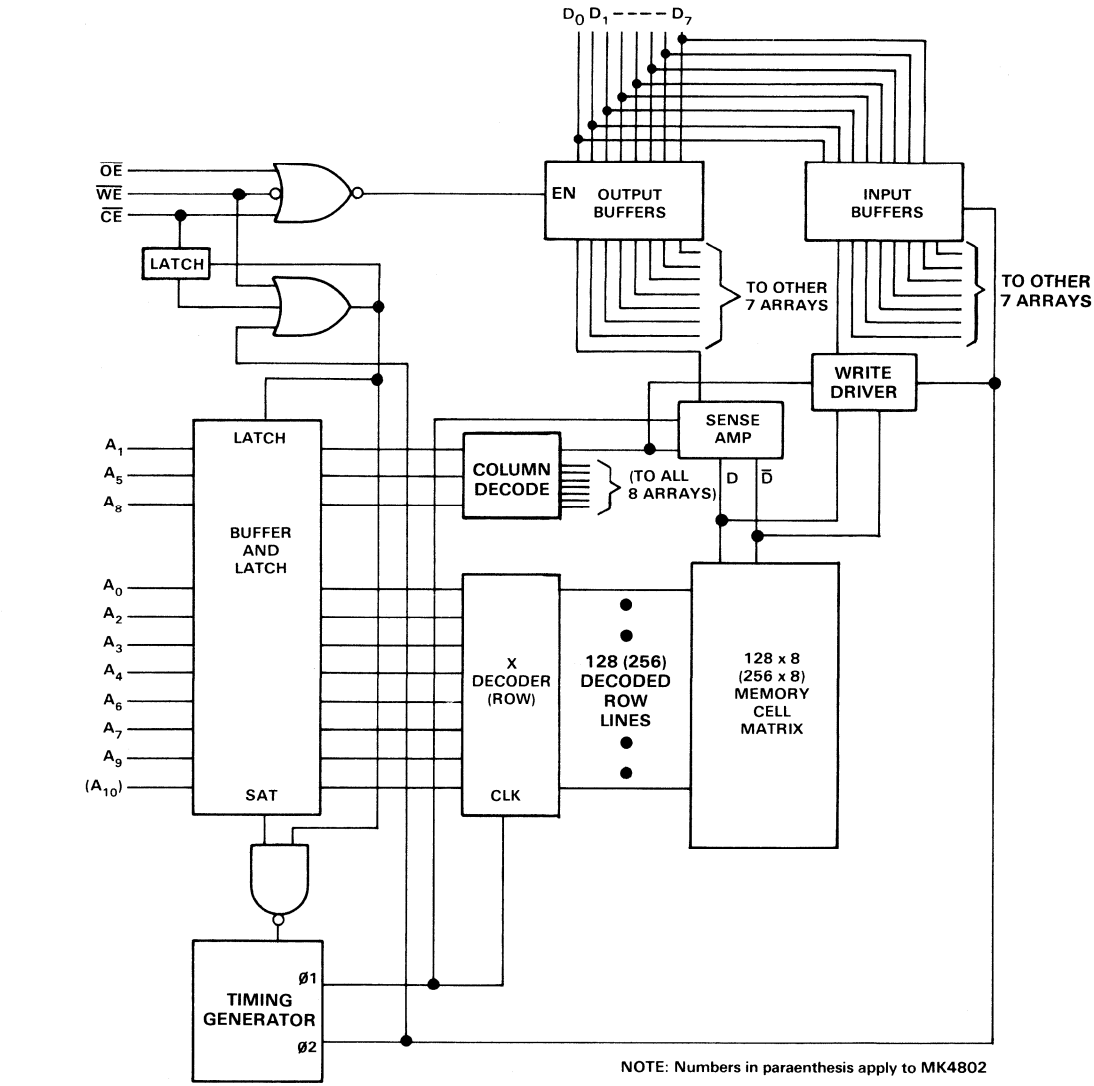
Figure 7

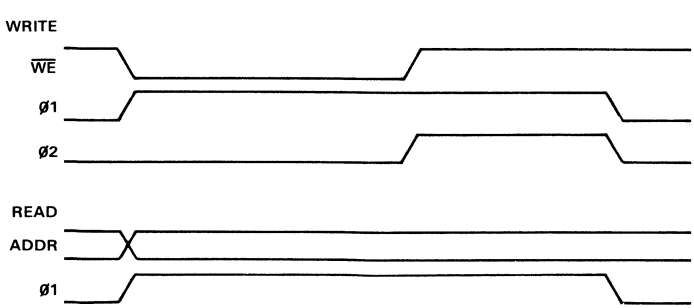


Device operating at 250ns period
Fully static reads accessing in ~ 70ns (OE = CE = O)

LOGIC DIAGRAM

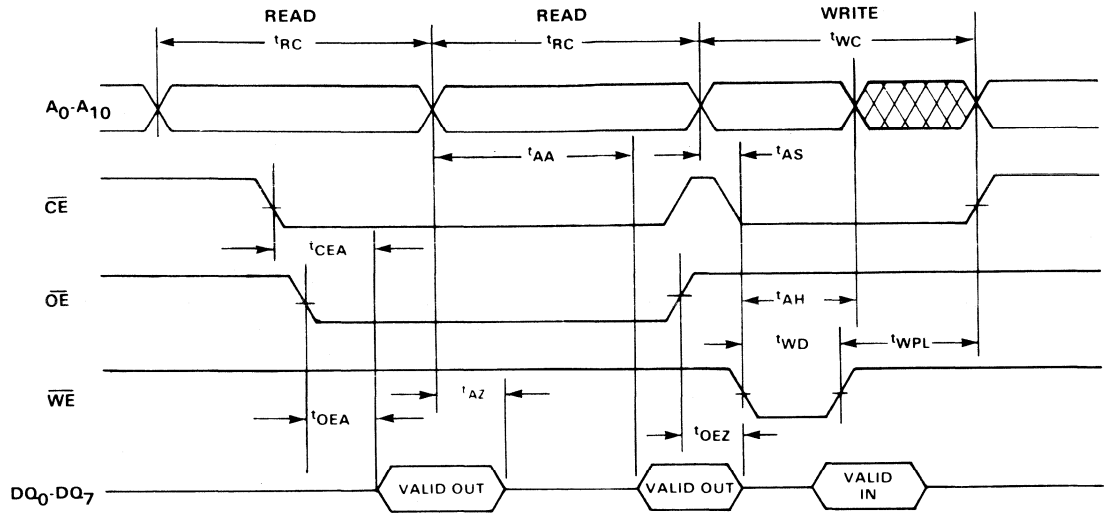
Figure 8





TIMING DIAGRAM

Figure 9



$\overline{OE}$ have been brought low within their access times, a single transition will occur at the outputs from the high impedance state to valid data. It should be noted that while Ø1 is active, the output buffers are disabled, guaranteeing a high impedance output. When address transitions occur before the completion of the access, the Ø1 cycle will not be completed, a new access will begin, and the outputs will remain in the high impedance state.

The advantage of an address activated read cycle is basically one of speed. As any system application would show, time is required to decode some of the highest order address lines into the $\overline{CE}$ signal. If chip access time begins from address transition instead of from the edge of $\overline{CE}$, then the chip decode time no longer needs to be minimized allowing the use of slower logic while speeding up system operation.

EDGE ACTIVATED™ WRITE

The consideration alluded to earlier causing the write cycle to operate differently from the read is basically one of data security. System noise during a read may abort a cycle, but it will not cause loss of data.

A simple example shows this need. If a write cycle were to operate the same as a read, and noise coupled into one of the address lines halfway through the Ø1 period, the write would be aborted potentially leaving the 8 cells in indeterminate states. So protective measures have been taken on the chip to eliminate this possibility.

Referring again to Figure 8, as soon as both $\overline{WE}$ and $\overline{CE}$ become active a signal is generated which latches up the status of the address inputs. It also marks the beginning of the familiar Ø1 clock. For a time referred to as t_{WD}, the row and column decoders are selecting the cell in each matrix to be written into and for t_{DSW} the data present at the I/O port is settling in the input buffers. When $\overline{WE}$ goes from low to high, the actual write process begins. At this point the Ø2 clock goes active preventing any activity on $\overline{CE}$ or $\overline{WE}$ from interfering with the completion of the write cycle. The Ø2 clock also enables the write drivers, which force the data and $\overline{data}$ lines for the selected column line to the cell input transistors, writing the cell. Then at the completion of Ø2, both Ø1 and Ø2 go low, allowing the start of a new cycle.

The ability to latch the status of the address and control lines during a read cycle was built into the slower MK4118, as well as the original MK4801 via a Pin 19 control function called $\overline{L}$. However, since this interferes with interchangeability with the MK4802, which has A10 on Pin 19, a No Connect was placed on that pin and an "A" was added to their part numbers resulting in the new designations of MK4118A and MK4801A.

LONGER WRITE

A quick glance at the data sheets reveals that for the -55, -70, and -90 parts, the write cycle is rated at 65ns, 80ns,

and 100ns respectively. This 10ns difference between the read and write cycles reflects realistic system constraints. Inside the parts, access time is determined by the Ø1 clock, which is the same for both types of cycles. However, a bi-directional data bus imposes some important timing considerations with respect to a read followed by a write and a write followed by a write. For this reason, the data sheets reflect this timing difference and show all combinations of cycles to increase the system engineer's awareness.

The 10ns difference is due to the time required to turn off the output buffers on the part following a read cycle. If the full 20ns following the $\overline{CE}$ line going high is used by a MK4801A-70 prior to the data bus going into the high impedance mode and is added to the data setup time of 5ns with another 5ns allowed for transitions, a write pulse duration of 30ns results. Referring to Figure 9, a write pulse lead time of 50ns is required for the write cycle to reach completion, resulting in a cycle time of 30ns + 50ns = 80ns in a -70 part.

This 10ns situation does not exist on MK4802s rated at slower than 100ns since there is more opportunity to absorb this 10ns within the guaranteed write pulse lead time t_{WPL}. In fact, on the MK4802-1 and the MK4802-3, $t_{WP} + t_{WPL}$ do not add up to t_{WC}, but add up to 10ns less.

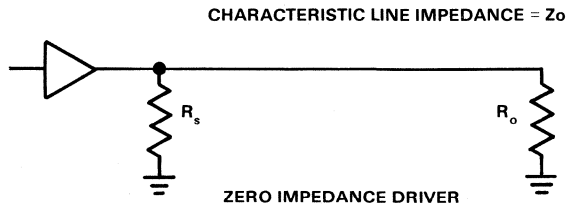
Success in designing high speed memory systems is closely tied to the attention given to analyzing delays through peripherials and other timing problems on the order of 5ns or 10ns. When such short times are of importance, transmission line effects start to enter into the picture and need to be considered as such to obtain the maximum system importance.

DRIVING AND TERMINATING

As system speeds increase, the design of the memory interface becomes much more than simply picking up an IC manufacturer's data book and selecting parts. Cycle times below 100ns require that every nanosecond available be usable by the parts, and not eaten up in propagation delays and ringing. In order to keep this wasted time to a minimum, a basic appreciation for the behavior of high frequency signals on a P.C. board needs to be obtained and this behavior needs to be accounted for.

When the propagation delay of an interconnection becomes significant with respect to the rise and fall times of the driver, the circuit enters the realm of transmission lines. If these effects are not considered, soft errors resulting from noise are possible. Some of these effects were looked at on a memory board which had been designed to exercise these memories. This was a 4 layer P.C. board with internal power and ground planes employing .020 line and spacing rules. Propagation delays of around 4 nanoseconds per foot were measured on this board, and since a row of 16 devices is 12 inches long, the propagation delays encountered are large compared to the 5ns desired rise and fall times.

IDEAL TRANSMISSION LINE
Figure 10



The ideal transmission line could be characterized as shown in Figure 10. When a zero impedance driver drives a line with a constant impedance of Zo into a matched termination with Ro=Zo, all of the energy sent down the line will be absorbed at Ro. However, memory systems are rarely ideal in nature and trade-offs must be made to keep reflections due to impedance mismatch from causing excessive ringing and undershoots. The top photo of Figure 11 shows that at the end of an unterminated transmission line undershoots of greater than -2V can result. The upper trace shows the signal measured at the schottky drivers output while the lower trace shows what is appearing at the end of the line. Mostek places a specification of -1.5V (for less than 50ns duration) as the minimum voltage on any pin, which this exceeds. However many manufacturers place a specification of -0.3V or -0.5V on undershoot. That makes proper termination all the more crucial.

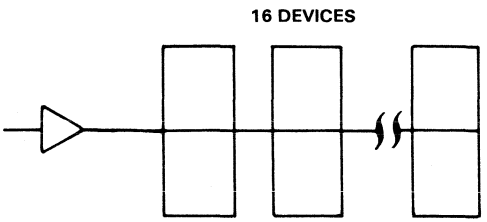
There are three commonly used techniques to rectify the undershoot problem. One of the simplist is a series resistor which serves to match the source impedance of the driver to the impedance of the P.C. trace. The second photo of Figure 11 demonstrates how well a 43Ω resistor attenuates that large undershoot found in the P.C. trace of the upper photo. Not only was the undershoot reduced but the noise on the line was also reduced without much degradation of the waveform. However since the PC trace has a characteristic impedance of around 80Ω some slight undershoot still results. The value of the series resistor can be empirically selected, however too large a resistor value will eliminate the undershoot at the expense of transition time and noise immunity.

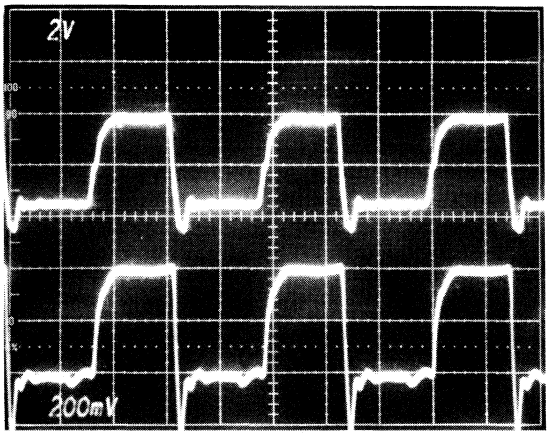
A second termination technique shifts the problem from the driver to the receiver. The series resistor used earlier is a form of reverse termination, allowing a single bounce from the impedance mismatch found when the PC trace ends. By properly terminating the end of the line, no reflection will occur resulting in a clean signal. But a simple 80Ω resistor placed at the end of the line presents an excessive DC load on the driver. Therefore, a capacitor is placed in series, allowing an AC termination into Zo and a DC open circuit to reduce loading. As can be seen in the third photo of Figure 11, undershoot is controlled on the line but the capacitor used is larger than may be required, restricting rise times. As suggested for the series resistor, R and C values can be selected empirically.

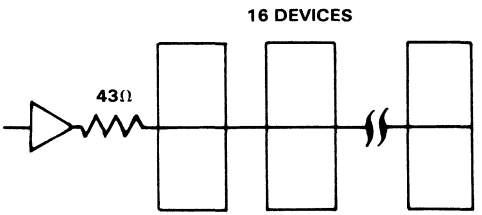
DRIVING THE ADDRESS BUS

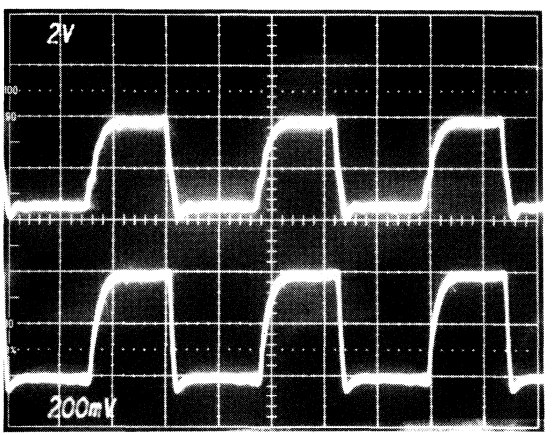
Figure 11

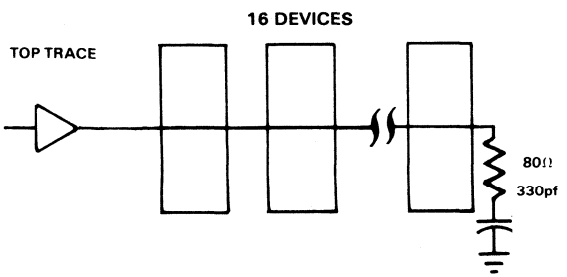
Vertical 2V/div
Horizontal 50ns/div

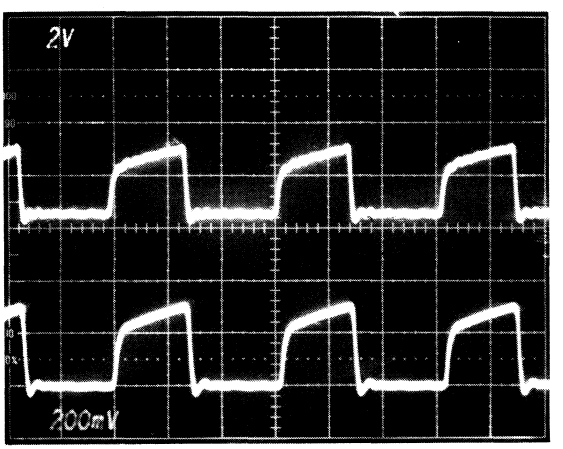










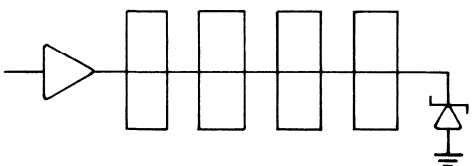


Driver - 8T97
Memories - MK4801A-90 16 pieces
Resistors - carbon composition
Capacitor - mica

Schottky diodes are also used as line terminators, although they handle the problem of undershoot in a more "brute force" manner. A forward biased schottky diode begins conducting at 0.3V, so a schottky diode placed as shown in Figure 12 should damp undershoots at -0.3V. But greater undershoots result due to the turn on times of real diodes. When a Hewlett Packard HSCH-1001 diode was placed at the end of the line used for the photos of Figure 11, the undershoots were damped at -1.0V. While this still leaves an undershoot, the diode will effectively limit it to a known value. Inputs on schottky TTL gates have a reversed biased schottky diode to the IC's substrate, but their turn on times are slower than the HSCH-1001's such that when used in the same example the undershoot was clamped at -1.6V.

TERMINATING THE LINE WITH A REVERSE BIASED DIODE

Figure 12



DRIVING THAT BIDIRECTIONAL BUS

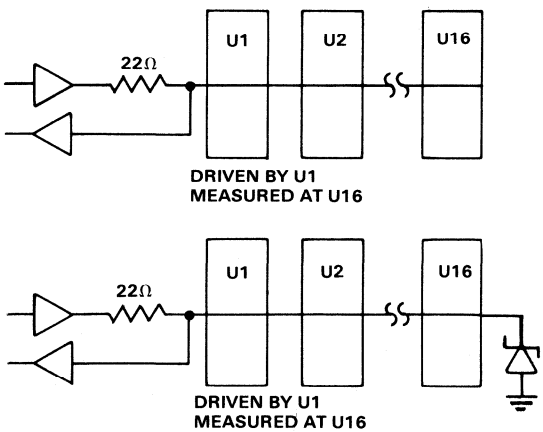
When considering the transmission line nature of a trace on a PC board, the example of a bidirectional data bus becomes very interesting. Not only is there a situation similar to a single driver driving a number of memory inputs, but each memory itself drives the line during a read cycle. This problem was analyzed on the same system as the address bus problem with the results shown in Figure 13.

A series resistor at the driver will handle the undershoot problem quite well when selected as previously discussed. However, when the driver is in a high impedance state the series resistor will not have a significant effect as a line terminator. Meanwhile, one of the memory devices will serve as a line driver. But MOS devices are not known as powerful line drivers and cannot compete for speed or low impedance when compared with a Schottky TTL device.

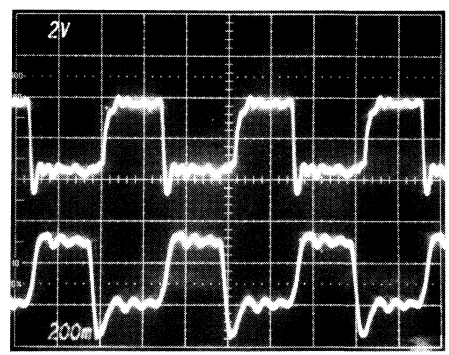
The scope photos in Figure 13 all show the address line in the upper trace which causes a read cycle to commence ($\overline{CE}$, $\overline{OE}$ low, $\overline{WE}$ high). The lower traces show the data line with the part operating at near its maximum speed (data transitions at or near the following address transition). The two photos have U1 driving the line, measuring the trace at U16. The lack of any form of termination causes an undershoot of -1.6V which exceeds Mostek's -1.5V for 50ns specification and it should be controlled. The second photo shows the damping effect of a schottky diode at U16, which limits the undershoot to a reasonable value.

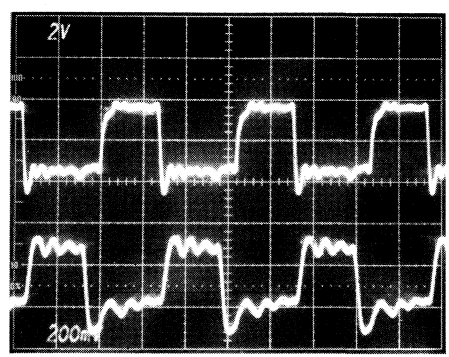
DRIVING THAT BIDIRECTIONAL BUS

Figure 13



Driver - 74LS244
Memories - MK4801A-90 16 pieces
Receiver - 74S153
Diode - HDSP 1001





Alternate terminations prove to be undesireable for the bidirectional bus. Series resistors at each device require excessive real estate, and a RC termination excessively loads down the MOS drivers.

PC LAYOUT - PLANNING AHEAD

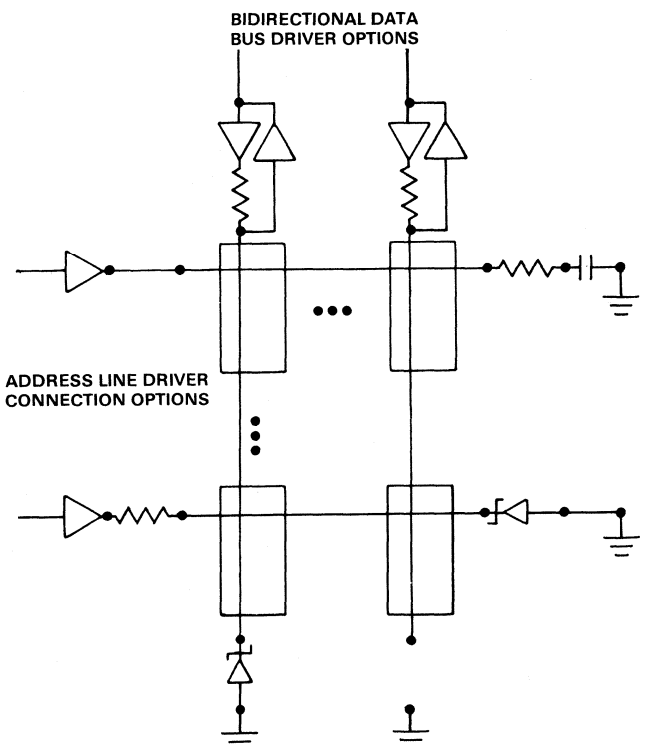
The choice of the type of termination, and the values to be used, depend on many variables. A limited number of these choices are viable options but the characteristics of printed circuit board traces vary enough that the selection of a specific combination of terminations should be delayed until a prototype can be characterized. If the resultant combination gives excessive undershoot or sluggish rise times, the selected values can be changed. Following are some suggestions for terminations, and Figure 14 shows a generalized memory array using these techniques.

1) Provice a series resistor in the address and control lines. Also provide for a R-C high frequency shunt at the end of the trace should it necessary. Generally one or the other of these will be selected.
2) Provide a series resistor at the data driver, but not between the data line and the receiver. When the resistor is between the data line and the receiver, the IR drop substracts from the noise margin. Also provide for a schottky diode at the end of the data line to provide termination when one of the memory devices is driving the line.

CONCLUSION

System designs can easily take advantage of the Bytewyde nature of the MK4801A/MK4802, but no system design in the sub 100ns speed is done without a high degree of care. Proper selection and design of the peripheral circuitry and proper layout of the array keeping traces short are vital to assure consistant performance, and these RAMs have been designed to make it easier. The wide word format, fast circuit operation, output enable control, Address Activated™ read, Edge Activated™ write, and ability to withstand -1.5V undershoots serve to make that system design easier. Cost has also been factored into the situation by virtue of the small die size. As manufacturing experience accumulates on these parts, a classical price reduction should occur making the MK4801A and the MK4802 more than competitive in the marketplace.

DESIGNING PC BOARDS WITH TERMINATOR OPTIONS
Figure 14



MOSTEK®

MOSTEK'S BYTEWYDE™ MEMORY PRODUCTS

Application Note

INTRODUCTION

The proliferation of low cost microprocessors has created many new opportunities and challenges. With evolvement of the microprocessor the need for specialized memory components has emerged. Mainframe memory designs of the past tended to be large in bit content with various word widths. Microprocessor memories, in contrast, are typically smaller in size with word widths fixed at X8 or X16 bits. This X8, or byte orientation, has given birth to wide word memories with new opportunities for standardization.

BYTEWYDE™ memories can adapt themselves to the microprocessor as building blocks because microprocessor architectures are byte oriented. By using these building blocks, memory design can inherit flexibility and compatibility that has not existed before. The design of custom memory arrays can be reduced to the mere insertion of components which directly match the microprocessor software requirements.

In memory design, various types of devices are more suited for a given application than others. The wide spread popularity of RAM, ROM, and EPROM validates the need for different types of memory devices. A truly non-volatile RAM could remove this complication. Since this device does not yet exist memory designers must decide, and usually very early in the design, how much and what type of memory components to use. Nevertheless a coherent memory packaging philosophy can resolve many problems associated with type, size, and expansion. The benefits of such an approach can be:

(1) RAM, ROM, EPROM interchange
(2) Upgradeability to higher density components
(3) Single component incremental expansion

ROM and PROM interchangeability has existed for some time. This convenience has been used with non-volatile memory to reduce memory cost after system confidence has been established by substituting ROM for EPROM in high volume applications. The availability of RAM with pin compatibility has furthered the process of interchangeability. Memory design, as a result, is less restrictive in that exact amounts of ROM vs RAM may be decided virtually after the design has been complete.

Socket upgradeability presupposes that a higher density part will exist and that the future part may be substituted for a former lower density part. Good memory designers will use the maximum density part available to reduce P.C. board space and cost; however, less clearly understood is that density of components doubles every 18 to 24 months. This seems to say with some certainty that a memory design which uses current state-of-the-art density will be out-dated in two years because of reduced cost effectiveness. However, many equipment manufacturers need 4 to 6 years of product life. Upgradeability allows not only the option for substituting new, higher density parts; but provides the solution to remaining price competitive. The wasteful practice of providing real estate consuming spare sockets for probable future development can be eliminated by allowing technology advances to provide expansion. Furthermore, a given matrix of memory can be populated to exact requirements with single component incremental expansion provided by BYTEWYDE organizations.

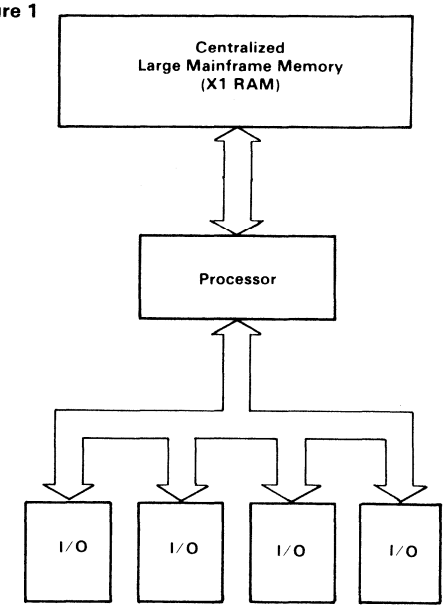
PACKAGE COMPATIBILITY

The 24 pin DIP has become the standard for presently available X8 memory devices. As the density of devices increases, more address pins will be needed to define higher density devices. This will create a need for future parts to occupy more than 24 pins. A logical choice is a 28 pin DIP package with the same pin spacing and package width differing only in the length occupied by the 4 additional pins. The key to future compatibility resides in the accepted 24 pin package pinout of today, and a 28 pin printed circuit board layout which is mutually inclusive of 24 and future 28 pin devices.

Mostek is dedicated to such an approach with its BYTEWYDE concept. This concept is particularly well suited for applications where the localized memory requirement can be implemented in 8 or less packages. Today, 80% of all 8 bit multi-chip microprocessor applications fall into this category. The future trend to distributed processor system architectures will emphasize smaller concentrations of memory localized in one area, although; the overall system requirement for memory will be substantial. Figure 1 shows the more traditional mainframe computer architecture of the 70's and Figure 2 shows the trend for the 80's using multiple microprocessors. Before proceeding to the packaging

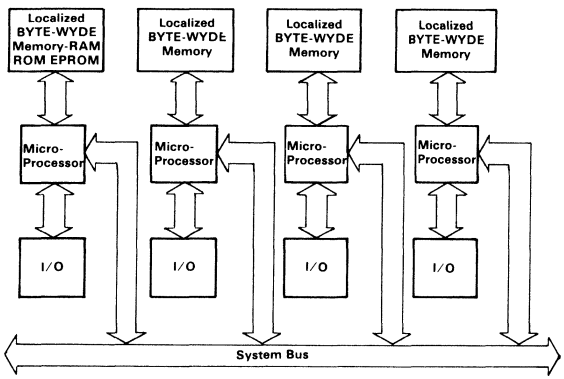
MAINFRAME COMPUTER ARCHITECTURE

Figure 1



MULTIPLE MICROPROCESSOR TREND OF THE 80's

Figure 2



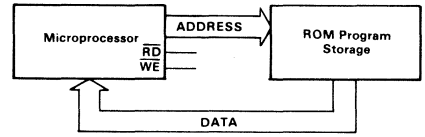
philosophy of BYTEWYDE memory control functions will be discussed.

MEMORY CONTROL FUNCTIONS

Memory control functions are provided to simplify interface and allow full utilization of performance. Historically, consistency in control functions has proved difficult. This is because control functions occupy pins which compete with address lines needed for future higher density parts. Three control functions have become very popular: chip enable, output enable, and write enable.

PROCESSOR/MEMORY INTERFACE - NO CONTROL FUNCTION

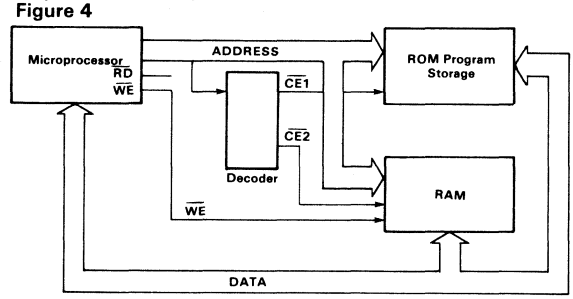
Figure 3



Insight into control functions can be gained by a few simple examples. The simplest case is a ROM processor interface in which addresses are supplied and data falls out at access time (Figure 3). No requirement for a control function is apparent. It is not until a second memory element is added that the need for the control function $\overline{CE}$ becomes evident (Figure 4). Since the microprocessor must now decide between the ROM and the other memory for a given access, some method must be provided to control device selection. The highest level selection control is called chip enable ($\overline{CE}$) by convention.

PROCESSOR/MEMORY INTERFACE - $\overline{CE}$, $\overline{WE}$ CONTROL

Figure 4



To reduce costly interconnects most microprocessors have a common data in and data out, many have addresses time multiplexed on this same bus. To avoid bus contention, a condition where two or more devices attempt to drive the common bus at the same time, the use of the output enable ($\overline{OE}$) memory control is often desirable.

PROCESSOR MEMORY INTERFACE $\overline{CE}$, $\overline{WE}$, $\overline{OE}$ CONTROL (MULTIPLEXED A/D BUS)

Figure 5

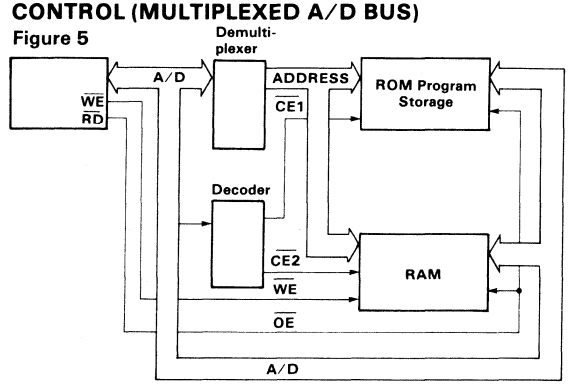


Figure 5 illustrates one of the many uses of an $\overline{OE}$ memory control. In this diagram the bus is time multiplexed, first with address then with data out to accomplish a read cycle. As soon as addresses are valid, it is advantageous to start the read cycle; however, without an $\overline{OE}$ control the possibility exists that the memory can go low impedance before addresses clear the bus. With an $\overline{OE}$ control, data can be held off until the bus is clear of addresses and still not impair memory access time.

A third control function is required for RAM called write enable ($\overline{WE}$). It is used to differentiate between read and write cycles. To achieve RAM interchangeability with ROM and EPROM, provisions for a $\overline{WE}$ must be incorporated into the system design and device pinout.

Having shown the usefulness of $\overline{CE}$ and $\overline{OE}$, a more complete description will be given:

Chip Enable - A $\overline{CE}$ (active low signal) is used to single out a device which is to go into cycle. $\overline{CE}$ will typically be generated from a decoder which uses the high order address lines to uniquely select a memory device among the matrix of devices. The second aspect of the $\overline{CE}$ control is to power up the selected device from a standby mode. In the case of dynamic logic $\overline{CE}$ activates the internal clocks necessary to complete the cycle. Use of dynamic logic within the device makes substantial power saving possible and is widely accepted. This control is located in pin 18 of today's 24 pin DIPs.

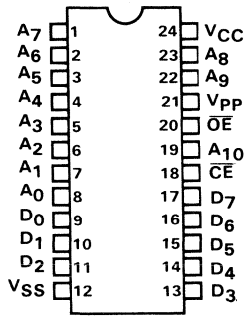
Output Enable - An $\overline{OE}$ (active low) controls the output buffer of the memory device. This control avoids bus contention since the memory device's output can be turned on and off directly by the controller (generally a microprocessor). Data can be gated out of the selected memory device ($\overline{CE}$ low to the selected device) at the precise time required. This control is located on pin 20 of today's 24 pin DIPs.

For many applications both $\overline{CE}$ and $\overline{OE}$ are needed to insure correct operation. The use of additional chip select signals ($\overline{CS}$) is viewed as redundant and serves little purpose, furthermore; it can cause compatibility problems with other memory device types. This also can have an adverse affect on upgradeability to next generation densities. If external decoding is needed, the sole advantage of additional chip selects is eliminated.

24 PIN PACKAGES

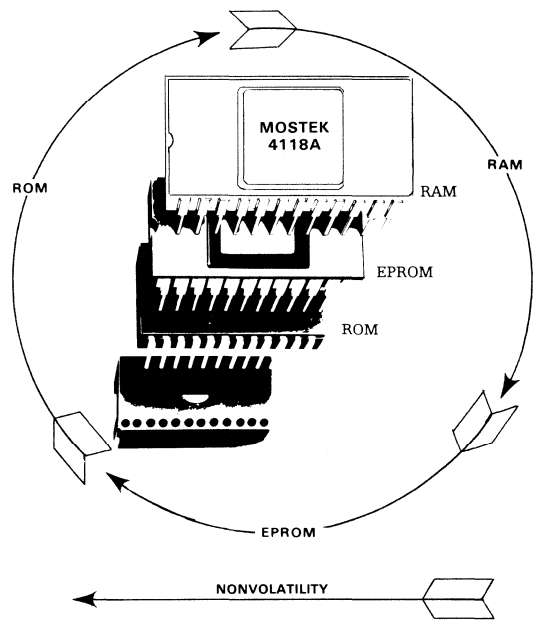
A good starting point for the discussion that will follow is the popular 2716 EPROM. The 2716 has found wide spread acceptance for microprocessor program storage. Figure 6 shows the 2716 pinout. Since this part is presently produced by no less than five manufacturers of memory devices, it may be safe to assume that this group has in itself agreed to standardization. Strengthening this assumption is the fact that many ROMs are available at the 2K level which are pinned to match the 2716.

2716 PINOUT - 2K x 8 EPROM
Figure 6



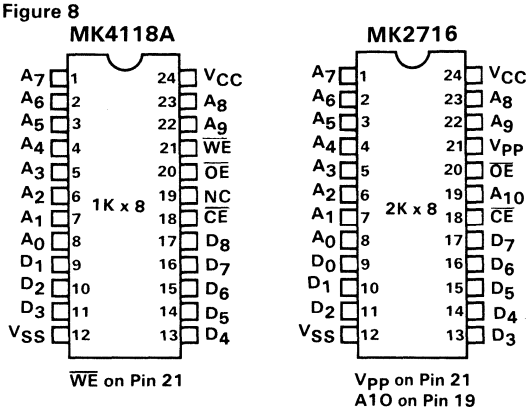
The MK4118A, 1K x 8 static RAM, packaged to the popular 2716 pinout, completes the compatibility circile (Figure 7). The 2716 is a 2K x 8 device requiring address line A10 as compared to the MK4118A, which is a 1K device. The MK4118A (Figure 8) will interchange with the 2716 if allowance is made for the write enable line ($\overline{WE}$) required on pin 21 by the MK4118A. The 2716, a ROM, does not required the write enable function. The availability of compatible 24 pin RAM, ROM and EPROM has completed the first phase of the BYTEWYDE concept.

TYPES OF MEMORY
Figure 7



COMPARISON PINOUT

Figure 8



FUTURE 28 PIN PACKAGING

Systems designers derive important benefits when component manufacturers discipline themselves to a well thought out packaging philosophy. The first phase of BYTEWYDE memory standardization and its packaging philosophy has already been achieved with the 24 pin package; however, the higher density memories of the future will required a 28 pin package and the proper planning to go along with it.

These principles should be used to guide the 28 pin package assignment:

(1) The popular 2716 pinout should be used to define address, data, $\overline{CE}$ and $\overline{OE}$.

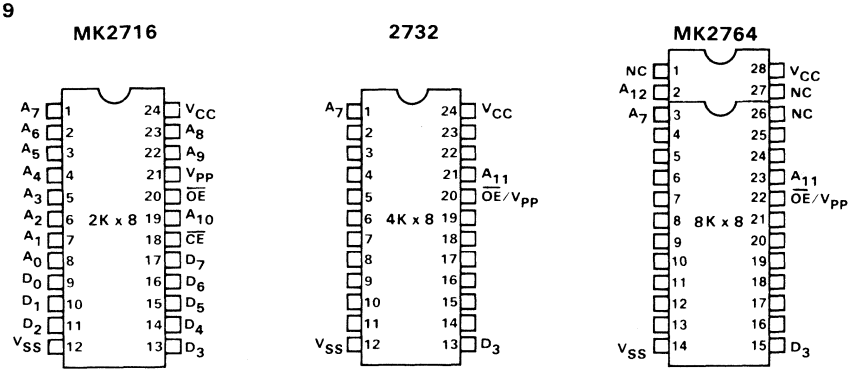
(2) 24 pin devices should coexist with 28 pin devices by lower justification. 24 pin devices are lower justified in pin 3 thru 26 of 28 pin socket.

(3) Consistent $\overline{CE}$ and $\overline{OE}$ control functions (same as 2716) should be used on all BYTEWYDE devices with provision for RAM ($\overline{WE}$).

(4) Spare pins at a given density level should be no connect rather than redundant chip selects ($\overline{CS}$) to allow for the ultimate development and upgradabiliy of 28 pin socket site.

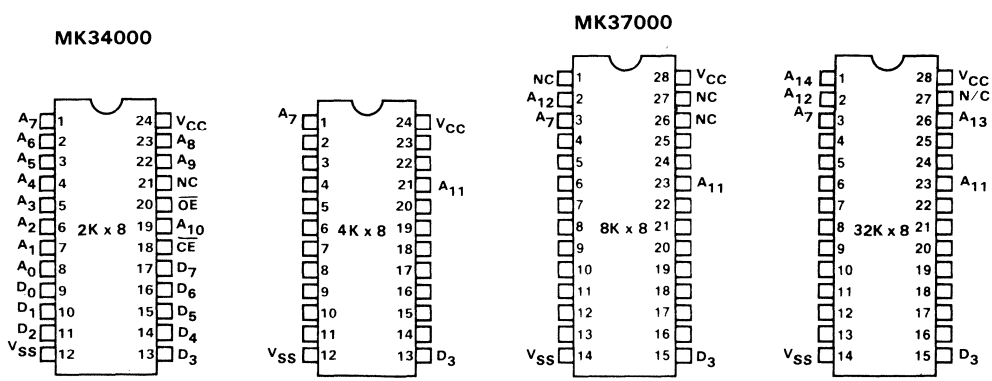
EPROM EVOLUTION

Figure 9



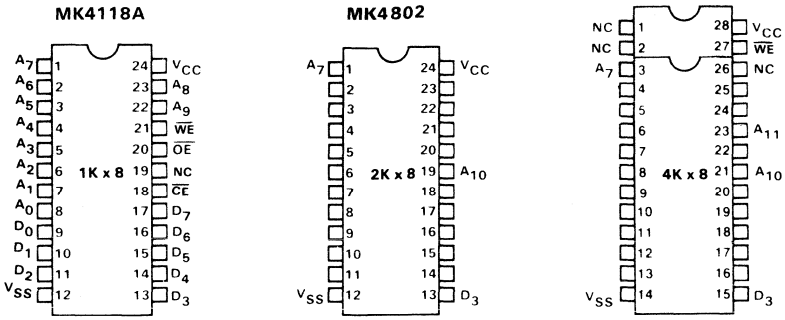
ROM EVOLUTION

Figure 10



STATIC RAM EVOLUTION

Figure 11



BYTEWYDE FAMILY PINOUTS

Figure 12

4118/A 4801A	4802	34000	2716	4K x 8	37000	32K x 8	2764		2764	32K x 8	37000	4K x 8	2716	34000	4802	4118A 4801A
				NC	NC	A14	NC	1 28	VCC	VCC	VCC	VCC				
				NC	A12	A12	A12	2 27	NC	NC	NC	WE				
A7	A7	A7	A7	A7	A7	A7	A7	3(1) (24)26	NC	A13	NC	NC	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6	A6	4(2) (23)25	A8	A8	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	A5	A5	5(3) (22)24	A9	A9	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	A4	A4	6(4) (21)23	A11	A11	A11	A11	VPP	NC	WE	WE
A3	A3	A3	A3	A3	A3	A3	A3	7(5) (20)22	OE/VPP	OE	OE	OE	OE	OE	OE	OE
A2	A2	A2	A2	A2	A2	A2	A2	8(6) (19)21	A10	A/O	A10	A/O	A10	A10	A10	NC
A1	A1	A1	A1	A1	A1	A1	A1	9(7) (18)20	CE	CE	CE	CE	CE	CE	CE	CE
A0	A0	A0	A0	A0	A0	A0	A0	10(8) (17)19	D7	D7	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	D0	D0	D0	11(9) (16)18	D6	D6	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	D1	D1	D1	12(10) (15)17	D5	D5	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	D2	D2	D2	13(11) (14)16	D4	D4	D4	D4	D4	D4	D4	D4
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	14(12) (13)15	D3	D3	D3	D3	D3	D3	D3	D3

Parenthesis Indicates Pin Number of 24 Pin Packages.
24 Pin Devices are Lower Justified in Pins 3 Thru 26 of 28 Pin Socket

With these issues in mind, Figure 9 shows EPROM evolution from 2K to 4K to 8K bytes. Figure 10 shows ROM evolution from 2K to 4K to 8K to 32K bytes. Figure 11 shows static RAM evolution from 1K to 2K to 4K bytes. Figure 12 shows the BYTEWYDE memory presently offered by Mostek.

Presently available 2K x 8 pseudostatic RAMs also fit the compatibility scheme mentioned with the exception of requiring an additional control function to determine refresh time. Pin 1 is presently being used by pseudostatic RAMs as the refresh control. This conflicts with some 8K x 8 EPROM proposals that use Pin 1 for V_{PP}. When V_{PP} is multiplexed with $\overline{OE}$, as in the case of the 2732, the problem is alleviated.

A new device on the horizon is called the E²PROM (Electrically Eraseable Programmable Read Only Memory). This part, when it is introduced, should produce some exciting and yet perplexing possibilities. As the name suggests, ultra-violet erasure is replaced by electrical erasure. The benefit of such a device would be in system programming and erasure. This intriguing idea could hold some hidden problems for BYTEWYDE memory standarization in that additional control functions and an in circuit high voltage pin would be required. It would be ideal if technology can solve this problem by the introduction time of these new devices so they could more closely emulate RAMs. Even if the pinout problem of E²PROM is solved, the interface to a microprocessor is likely to remain difficult because of slow write cycle and block erasure.

INTERFACE TO MICROPROCESSORS

The BYTEWYDE memories discussed can be interfaced easily to microprocessors. This fact will be reduced to practice demonstrated by a microprocessor/memory interface using eight socket memory matrix example.

Memory design goals:

(1) RAM, ROM, EPROM interchange

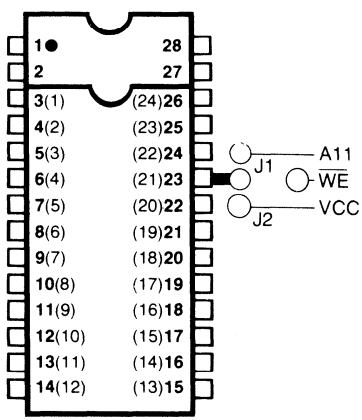
A. Program storage during software debug using RAM

B. Program storage during prototype production using EPROM
C. Program storage during production using ROM

(2) Ratio of RAM/ROM flexible to allow for changing system requirements
(3) Minimized package count (density and testing consideration)
(4) Memory expansion capability for after market system enhancements
(5) Minimum granularity for memory expansion in small increments
(6) Memory design to stay cost effective for product life 4-6 years
(7) System throughput not be limited by memory performance
(8) Multiple sources for RAM, ROM, EPROM
(9) Initial estimate of memory requirements 4K RAM 4K EPROM (non-volatile program storage)

JUMPER ARRANGEMENT FOR RAM/ROM INTERCHANGE

Figure 13 **JUMPER LAYOUT**



The first step is to design a memory matrix to accomodate RAM, ROM, and EPROM. Since pinout compatibility exists, eight identical 28 pin sockets will be used. The only special consideration which must be made is a jumper for pin 23, to allow for RAM/ROM compatibility (see Figure 13). Pin 23 connection will be jumpered to the write enable signal ($\overline{WE}$) for 1K and 2K RAMs, to A11 for ROMs, EPROMs or RAMs larger than 2K, or +5 for 2K EPROMs. All other control, address, and data lines are bussed together with the exception of the chip enable lines ($\overline{CE}$). These connections must be individually routed to the decoder circuitry.

To define the address space of a particular socket site, a 256 x 4 PROM will be used for the $\overline{CE}$ decode of four sockets. The PROM decoder provides the flexibility of selecting from 1K to 32K bytes of memory at each socket location and can be also used to implement byte addressability for 16 bit microprocessors.

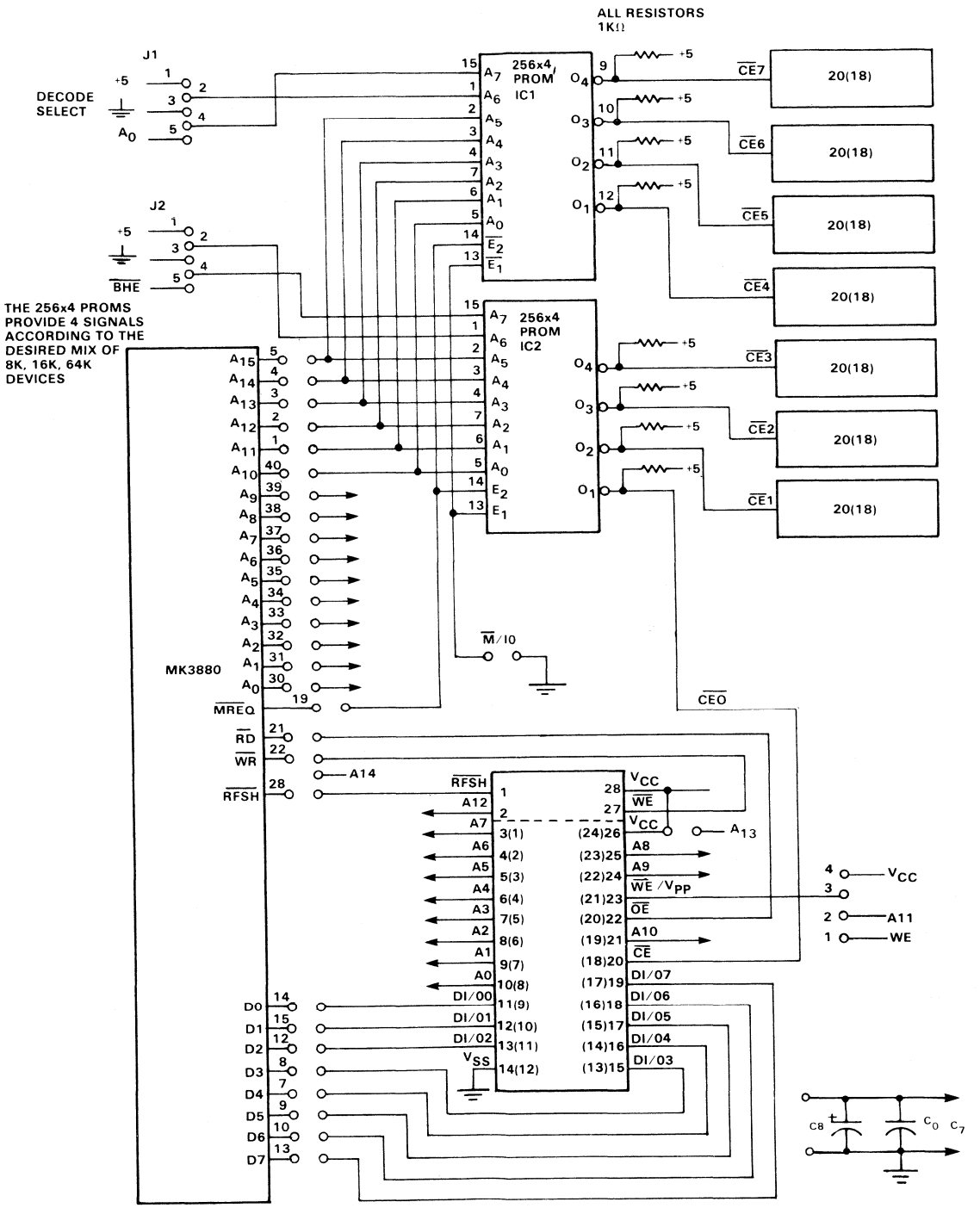
The microprocessor can now be connected directly to the memory matrix (see Figure 14). In this example, a 3880/Z80 microprocessor is used; however, many other microprocessors can be substituted.

CONCLUSION

RAM, ROM, EPROM interchange, consistent control functions, a coherent packaging philosophy, future density upgradeability without redesign, and memory expansion by addition of a single device make BYTEWYDE memory a natural selection for new microprocessor memory design. The standardization of BYTEWYDE memory can eliminate many problems imposed by ever changing software and heretofore rigid memory configurations. BYTEWYDE is a concept for the future which makes sense today. Alternative approaches have shortcomings which cause them to be less cost effective. Dynamic RAMs with x1 organizations are meaningful for large memory but inappropriate as a building block for smaller microprocessor memory. Static RAM like the 2114 1K x 4 require higher package count, offer no upgrade potential, and lack compatibility with ROM/EPROM. The printed circuit board density achieveable using BYTEWYDE memory is equivalent to the alternative approaches today and will be superior in the future without redesign. Memory cost is minimized by the increased engineering return on investment and economics to scale associated with prolonged usage of the same design.

INTERFACE TO AN MK3880

Figure 14



MOSTEK®

1K x 8-BIT STATIC RAM

MK4118A(P/J/N) Series

FEATURES

- ☐ Static operation
- ☐ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ High performance
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

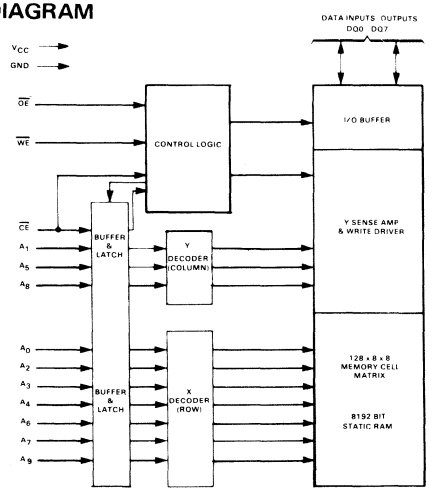
Part No.	Access Time	R/W Cycle Time
MK4118A-1	120 nsec	120 nsec
MK4118A-2	150 nsec	150 nsec
MK4118A-3	200 nsec	200 nsec
MK4118A-4	250 nsec	250 nsec

DESCRIPTION

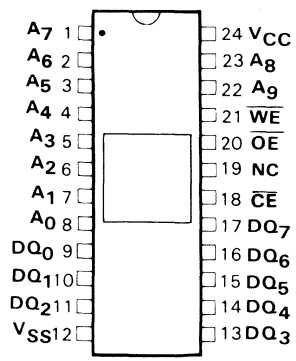
The MK4118A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4118A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4118A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to +7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[8]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 10

DC ELECTRICAL CHARACTERISTICS[1,8]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	9
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10pF		6,7

ELECTRICAL CHARACTERISTICS [3,4]

($0°C \leq T_A \leq 70°$) (V_{CC} = 5.0 volts ± 5%)

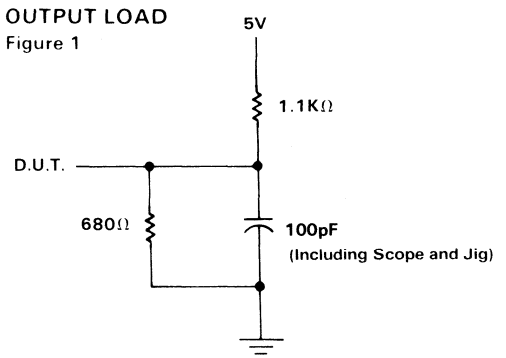
		MK4118A-1		MK4118A-2		MK4118A-3		MK4118A-4			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	5
t_{CEA}	Chip Enable Access Time		60		75		100		125	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	5
t_{OEZ}	Output Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	see text
t_{AH}	Address Hold Time	40		50		65		80		ns	see text
t_{DSW}	Data To Write Setup Time	10		10		15		20		ns	
t_{DHW}	Data From Write Hold Time	15		20		25		30		ns	
t_{WD}	Write Pulse Duration	45		50		60		70		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

NOTES

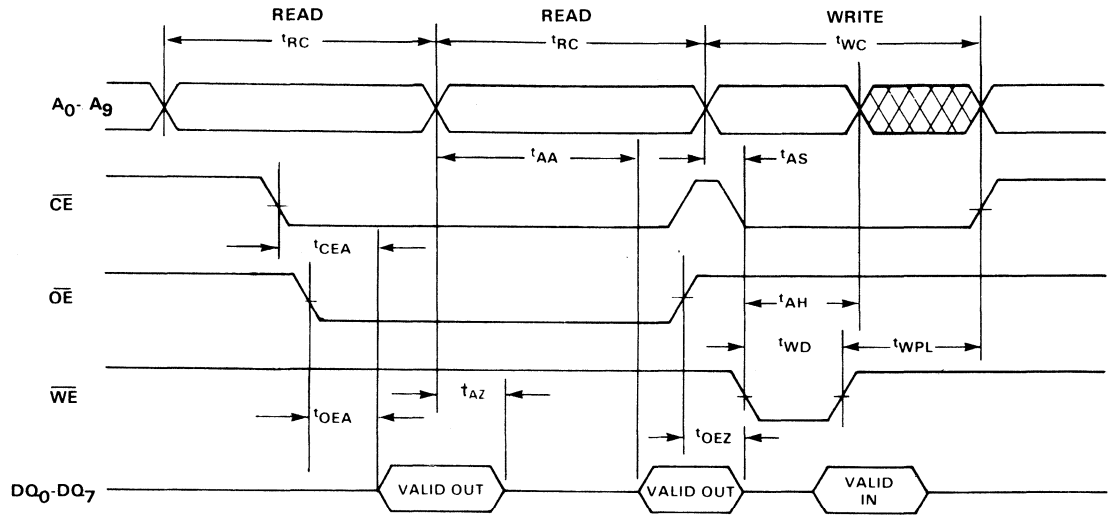
1. All voltages referenced to V_{SS}
2. Measured with $.4 \leq V_I \leq 5.0V$, outputs deselected and V_{CC} = 5V
3. AC measurements assume Transition Time = 5ns levels V_{SS} to 3.0V
4. Input and output timing reference levels are at 1.5V
5. Measured with a load as shown in Figure 1
6. Effective capacitance calculated from the equation $C = \frac{\triangle Q}{\triangle V}$ with $\triangle V$ = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected
8. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
9. I_{CC} measured with outputs open.
10. Negative undershoots to a minimum of -1.5V are allowed with a maximum of 50ns pulse width.

OUTPUT LOAD

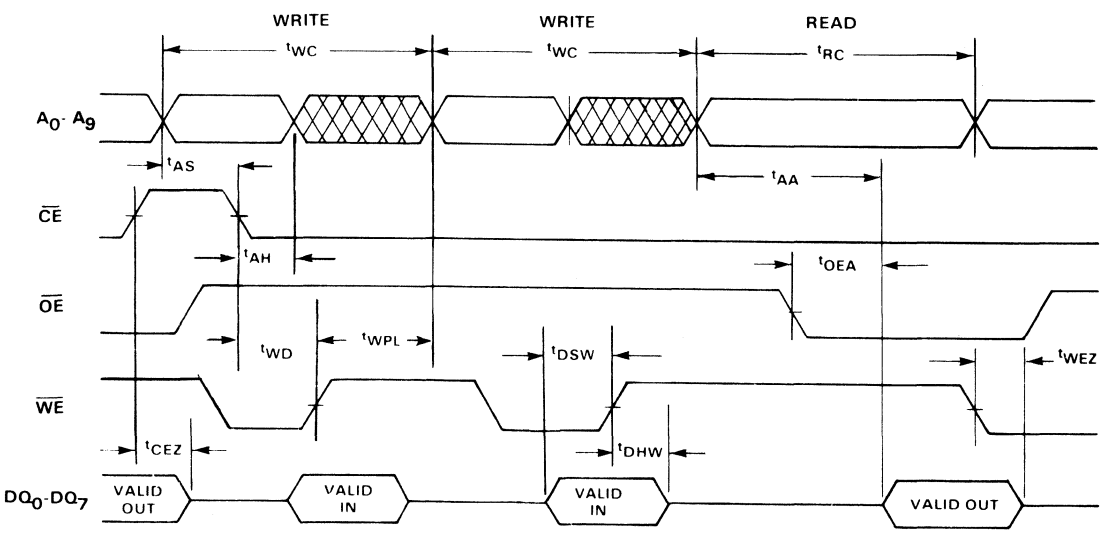
Figure 1



TIMING DIAGRAM
Figure 2



TIMING DIAGRAM
Figure 3



The MK4118A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4118A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs. Mostek also offers a higher performance version of the MK4118A designated the MK4801A.

READ MODE

The MK4118A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4118A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MK4118A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4118A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

PRELIMINARY

MOSTEK®

1K x 8-BIT STATIC RAM

MK4801A(P/J/N) Series

FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- High performance
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

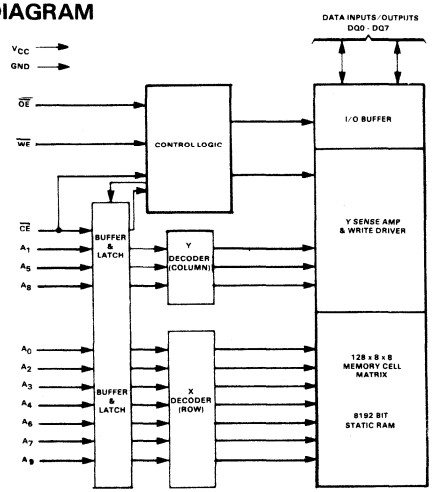
Part No.	Access Time	R/W Cycle Time
MK4801A-70	70 nsec	70/80 nsec
MK4801A-90	90 nsec	90/100 nsec

DESCRIPTION

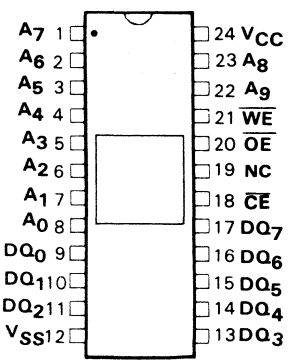
The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to + 7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[8]

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1,10

DC ELECTRICAL CHARACTERISTICS[1,8]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		125	mA	9
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-50	50	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10pF		6,7

ELECTRICAL CHARACTERISTICS [3,4]

($0°C \leq T_A \leq 70°$) (V_{CC} = 5.0 volts ± 5%)

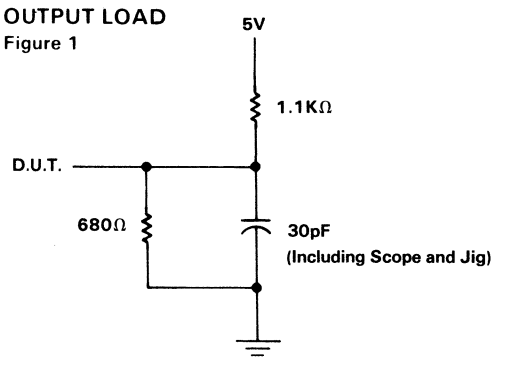
SYM	PARAMETER	MK4801A-70		MK4801A-90		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	70		90		ns	
t_{AA}	Address Access Time		70		90	ns	5
t_{CEA}	Chip Enable Access Time		35		45	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	20	5	30	ns	
t_{OEA}	Output Enable Access Time		35		45	ns	5
t_{OEZ}	Output Enable Data Off Time	5	20	5	30	ns	
t_{AZ}	Address Data Off Time	10		10		ns	
t_{WC}	Write Cycle Time	80		100		ns	
t_{AS}	Address Setup Time	0		0		ns	see text
t_{AH}	Address Hold Time	20		30		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		ns	
t_{DHW}	Data From Write Hold Time	10		10		ns	
t_{WD}	Write Pulse Duration	30		40		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	15	5	25	ns	
t_{WPL}	Write Pulse Lead Time	50		60		ns	

NOTES:

1. All voltages referenced to V_{SS}
2. Measured with $.4 \leq V_I \leq 5.0V$, outputs deselected and V_{CC} = 5V
3. AC measurements assume Transition Time = 5ns levels V_{SS} to 3.0V
4. Input and output timing reference levels are at 1.5V
5. Measured with a load as shown in Figure 1
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected
8. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
9. I_{CC1} measured with outputs open.
10. Negative undershoots to a minimum of -1.5V are allowed with a maximum of 50ns pulse width.

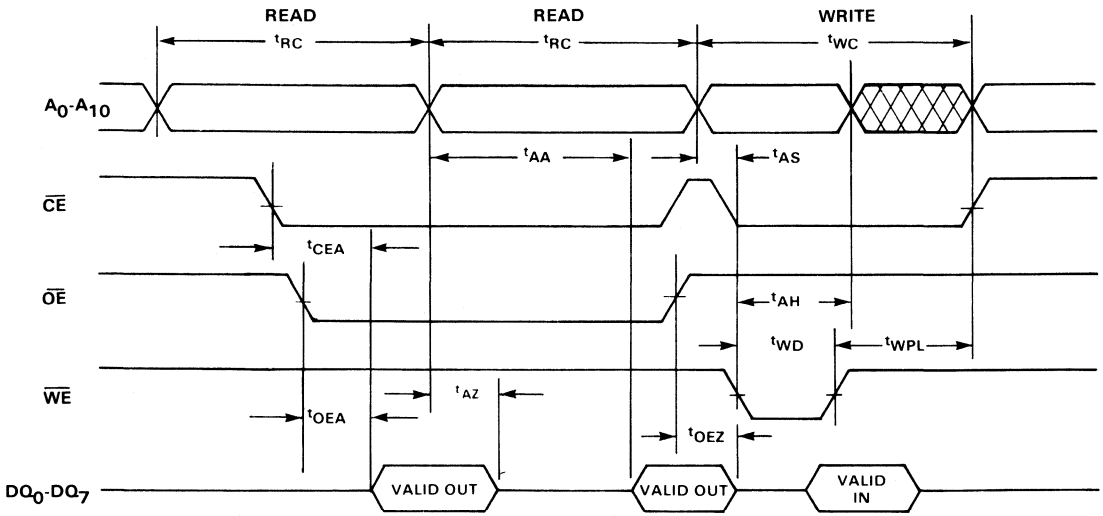
OUTPUT LOAD

Figure 1



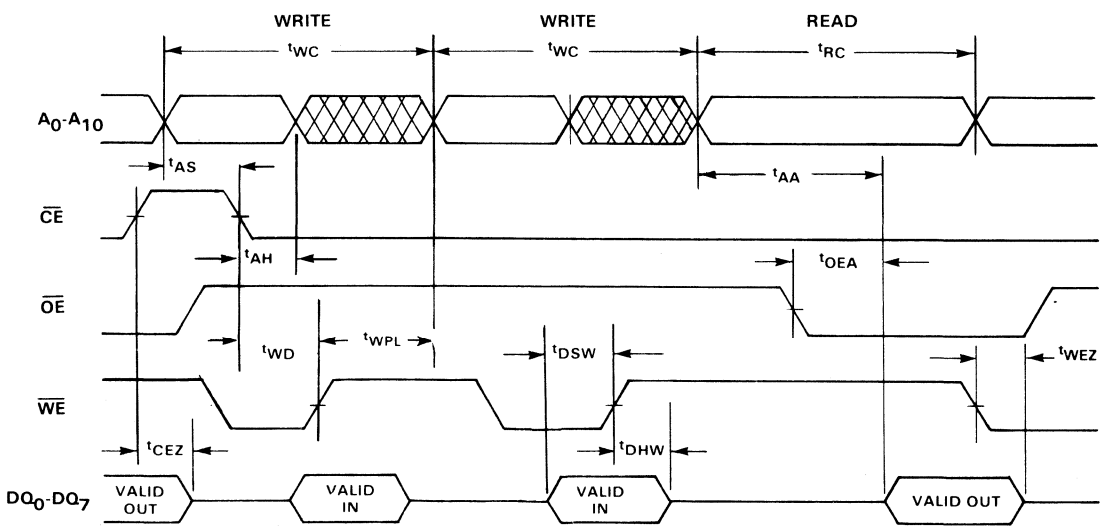
TIMING DIAGRAM

Figure 1



TIMING DIAGRAM

Figure 2



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

READ MODE

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.
In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

PRELIMINARY

MOSTEK

2K x 8 STATIC RAM

MK4802(P/J/N) Series

FEATURES

- ☐ Static operation
- ☐ Organization: 2K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ Double density version of the MK4118 1K x 8 static RAM
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- ☐ High performance

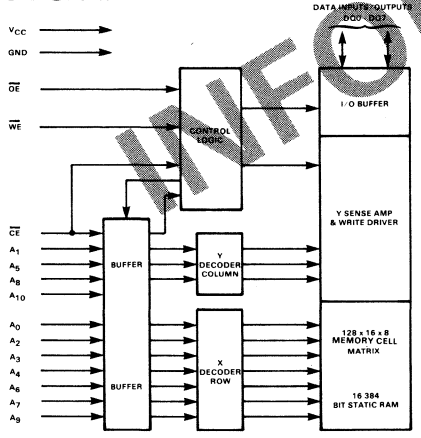
Part No.	Access Time	R/W Cycle Time
MK4802-70	70 nsec	70/80 nsec
MK4802-90	90 nsec	90/100 nsec

DESCRIPTION

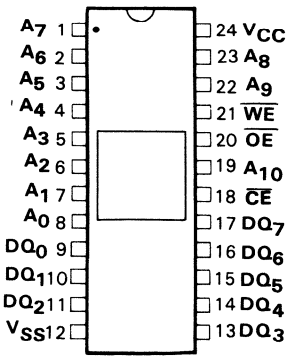
The MK4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4802 excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4802 presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory. The slower MK4802-3* provides even greater economies with performance suitable for microprocessor memory requirements.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

*See MK4802-3 Data Sheet

PIN NAMES

A_0-A_{10}	Address Inputs	V_{CC}	Power (+5V)
$\overline{CE}$	Chip Enable	$\overline{WE}$	Write Enable
V_{SS}	Ground	$\overline{OE}$	Output Enable
DQ_0-DQ_7	Data In/Data Out		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to + 7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS[8]

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		V_{CC} + .5V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1,10

DC ELECTRICAL CHARACTERISTICS[1,8]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		125	mA	9
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-50	50	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10pF		6,7

ELECTRICAL CHARACTERISTICS[3,4]

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 volts ± 5%)

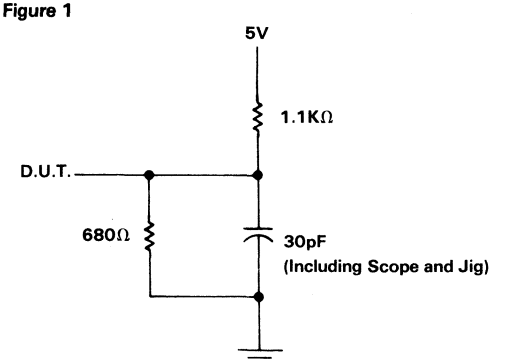
SYM	PARAMETER	MK4802-70		MK4802-90		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	70		90		ns	
t_{AA}	Address Access Time		70		90	ns	5
t_{CEA}	Chip Enable Access Time		35		45	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	20	5	30	ns	
t_{OEA}	Output Enable Access Time		35		45	ns	5
t_{OEZ}	Output Enable Data Off Time	5	20	5	30	ns	5
t_{AZ}	Address Data Off Time	10		10		ns	
t_{WC}	Write Cycle Time	80		100		ns	
t_{AS}	Address Setup Time	0		0		ns	see text
t_{AH}	Address Hold Time	20		30		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		ns	
t_{DHW}	Data From Write Hold Time	10		10		ns	
t_{WD}	Write Pulse Duration	30		40		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	15	5	25	ns	
t_{WPL}	Write Pulse Lead Time	50		60		ns	

NOTES:

1. All voltages referenced to V_{SS}
2. Measured with $.4 \leq V_I \leq 5.0V$, outputs deselected and V_{CC} = 5V
3. AC measurements assume Transition Time = 5ns levels V_{SS} to 3.0V
4. Input and output timing reference levels are at 1.5V
5. Measured with a load as shown in Figure 1
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected
8. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
9. I_{CC1} measured with outputs open.
10. Negative undershoots to a minimum of -1.5V are allowed with a maximum of 50ns pulse width.

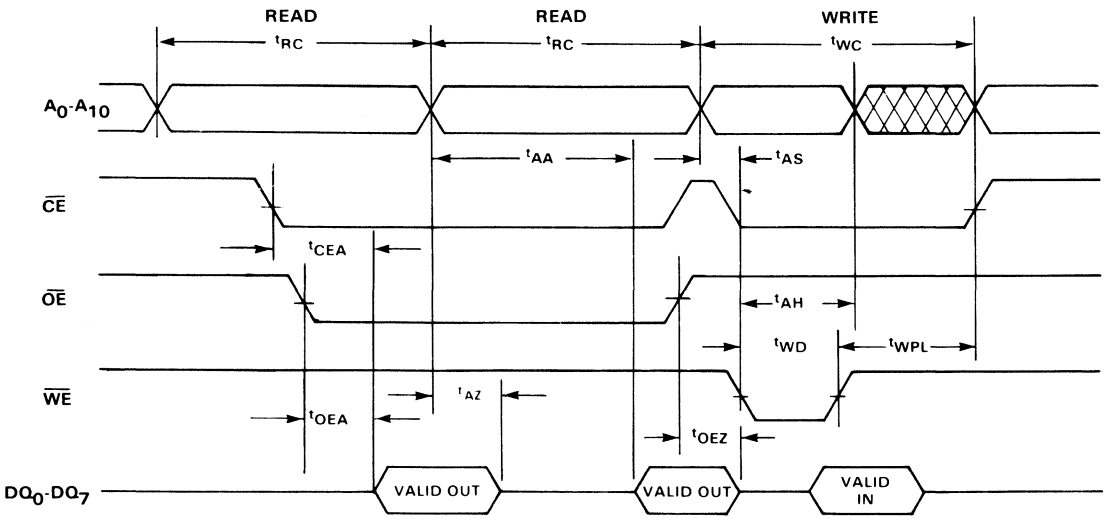
OUTPUT LOAD

Figure 1



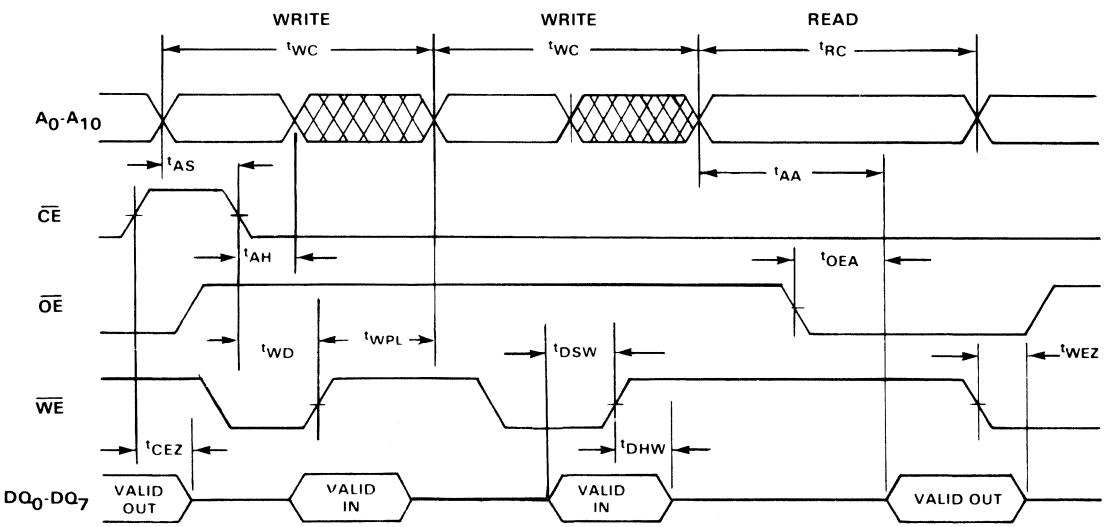
TIMING DIAGRAM

Figure 1



TIMING DIAGRAM

Figure 2



The MK4802 features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4802 is pin compatible with Mostek's BYTEWYDE™ Memory Family of RAMs, ROMs and EPROMS.

OPERATION

READ MODE

The MK4802 is in the READ MODE whenever the Write Enable Control Input ($\overline{WE}$) is in the high state. In the READ mode of operation, the MK4802 provides a fast address ripple-through access of data from 8 of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which 1 of 2048 bytes of data is to be accessed.

A transition on any of the 11 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MK4802 is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4802 disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

PRELIMINARY

MOSTEK®

2K x 8 STATIC RAM

MK4802(P/J/N)*-1/3

FEATURES

- ☐ Static operation
- ☐ Organization: 2K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ Double density version of the MK4118 1K x 8 static RAM
- ☐ 24/28 pin ROM/PROM compatible pin configuration

Part No.	Access Time	R/W Cycle Time
MK4802-1	120 nsec	120 nsec
MK4802-3	200 nsec	200 nsec

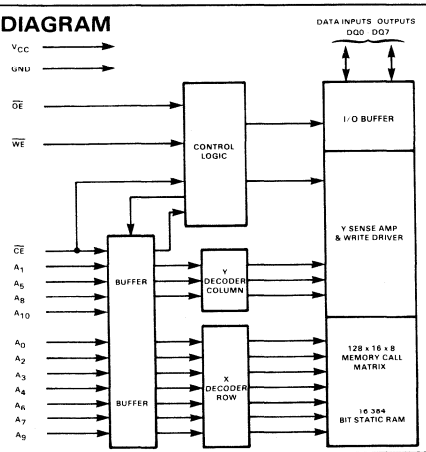
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

DESCRIPTION

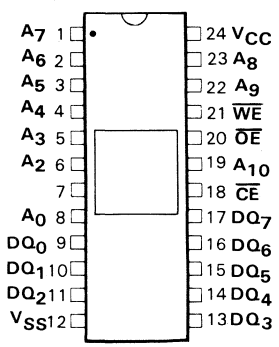
The MK4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

Both the MK4802-1 and MK4802-3 present to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's high performance microprocessor applications. The MK4802 is ideal for memory applications where the organization requires relatively shallow depth with a wide word format.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

*See MK4802 Series data sheet for faster speeds

PIN NAMES

A_0-A_{10}	Address Inputs	V_{CC}	Power (+5V)
$\overline{CE}$	Chip Enable	$\overline{WE}$	Write Enable
V_{SS}	Ground	$\overline{OE}$	Output Enable
DQ_0-DQ_7	Data In/Data Out		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS[8]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		V_{CC} + .5V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1,10

DC ELECTRICAL CHARACTERISTICS[1,8]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		125	mA	9
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT}=-1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT}=4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10pF		6,7

ELECTRICAL CHARACTERISTICS[3,4]

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 volts ± 5%)

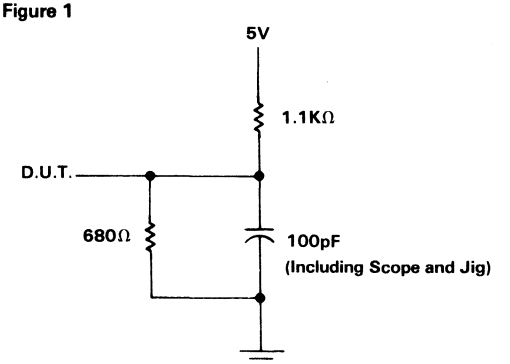
SYM	PARAMETER	MK4802-1		MK4802-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	120		200		ns	
t_{AA}	Address Access Time		120		200	ns	5
t_{CEA}	Chip Enable Access Time		60		100	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	30	5	35	ns	
t_{OEA}	Output Enable Access Time		60		100	ns	5
t_{OEZ}	Output Enable Data Off Time	5	30	5	35	ns	
t_{AZ}	Address Data Off Time	10		10		ns	
t_{WC}	Write Cycle Time	120		200		ns	
t_{AS}	Address Setup Time	0		0		ns	see text
t_{AH}	Address Hold Time	40		65		ns	see text
t_{DSW}	Data To Write Setup Time	10		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		ns	
t_{WD}	Write Pulse Duration	45		60		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	30	5	35	ns	
t_{WPL}	Write Pulse Lead Time	65		130		ns	

NOTES:

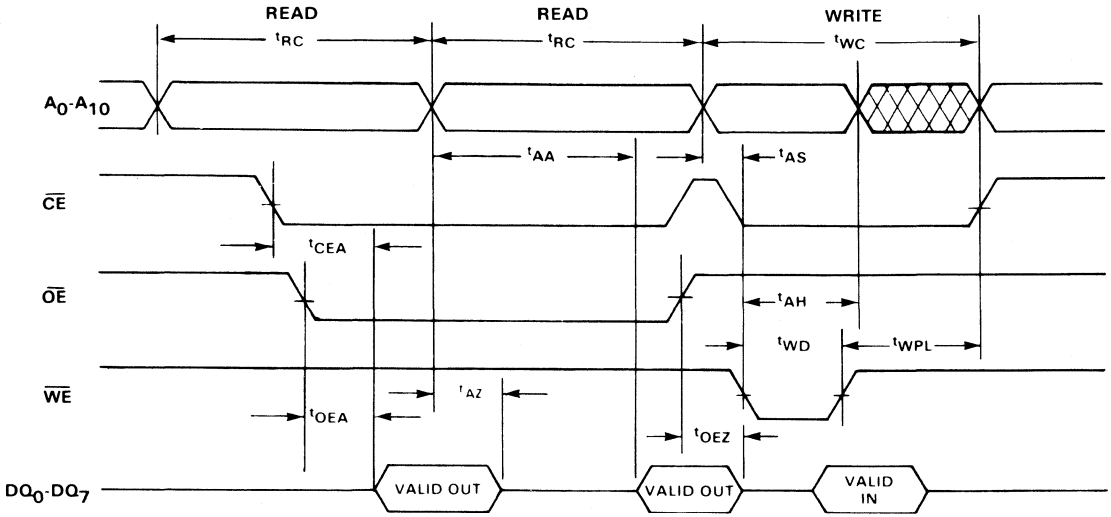
1. All voltages referenced to V_{SS}
2. Measured with $.4 \leq V_I \leq 5.0V$, outputs deselected and V_{CC} = 5V
3. AC measurements assume Transition Time = 5ns levels V_{SS} to 3.0V
4. Input and output timing reference levels are at 1.5V
5. Measured with a load as shown in Figure 1
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels
7. Output buffer is deselected
8. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved
9. I_{CC1} measured with outputs open
10. Negative undershoots to a minimum of -1.5V are allowed with a maximum of 50ns pulse width. DC value of low level input must not exceed -0.3V.

OUTPUT LOAD

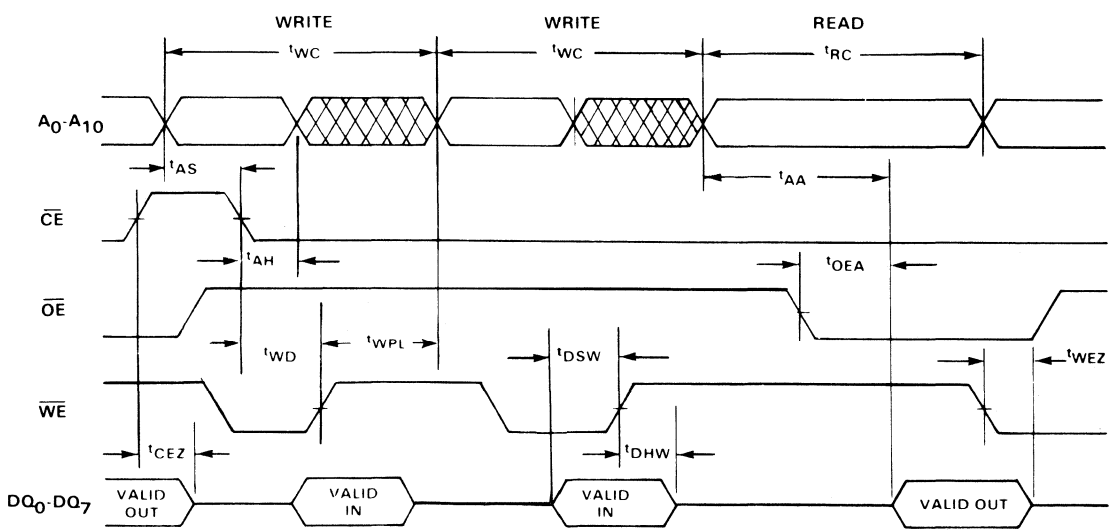
Figure 1



TIMING DIAGRAM
Figure 2



TIMING DIAGRAM
Figure 3



The MK4802 features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4802 is pin compatible with Mostek's BYTEWYDE™ Memory Family of RAMs, ROMs and EPROMs.

OPERATION

READ MODE

The MK4802 is in the READ MODE whenever the Write Enable Control Input ($\overline{WE}$) is in the high state. In the READ mode of operation, the MK4802 provides a fast address ripple-through access of data from 8 of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which 1 of 2048 bytes of data is to be accessed.

A transition on any of the 11 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MK4802 is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that CE is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) the $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4802 disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

MOSTEK®

2048 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (J)-5/6/7/8

FEATURES

- ☐ 16,384 Bit Ultraviolet Erasable, Electrically Programmable ROM, organized as 2048 words by 8 bits
- ☐ Single +5 volt power supply during READ operation
- ☐ Fast Access Time in READ mode

P/N	ACCESS TIME
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

- ☐ Low Power Dissipation: 525mW max active
- ☐ Power Down Mode: 132mW max standby
- ☐ Three State Output OR-tie capability
- ☐ Five modes of operation for greater system flexibility (see Table)
- ☐ Single programming requirement: single location programming with one 50msec pulse
- ☐ Pin Compatible with Mostek's BYTEWYDE™ Memory Family
- ☐ TTL compatible in all operating modes
- ☐ Standard 24 pin DIP with transparent lid

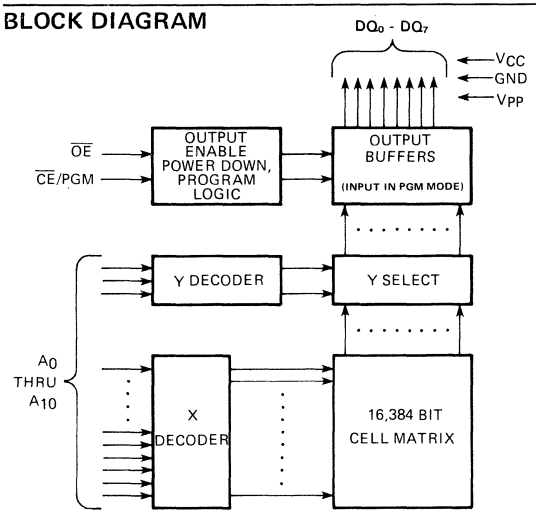
DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over

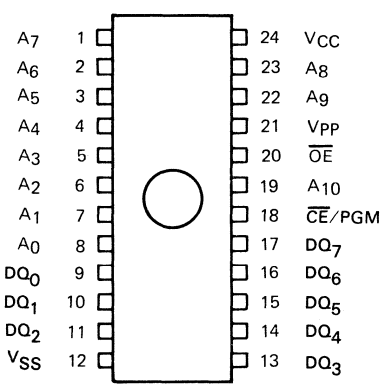
MODE SELECTION

MODE	$\overline{CE}$/PGM	$\overline{OE}$	VPP	OUTPUTS
PIN	(18)	(20)	(21)	
READ	V_{IL}	V_{IL}	+5	Valid Out
STANDBY	V_{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	Valid Out
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	Open
V_{CC}(24) = 5V all modes				

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Addresses	DQ_0-DQ_7	Data Outputs*
$\overline{CE}$/PGM	Chip Enable/ Program	$\overline{OE}$	Output Enable
		V_{SS}	Ground

*Inputs in Program Mode

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} (Except V_{PP}) ..... -0.3V to +6V
Voltage on V_{PP} supply pin relative to V_{SS} ..... -0.3V to +28V
Operating Temperature T_A (Ambient) ..... $0°C \leq T_A \leq 70°C$
Storage Temperature (Ambient) ..... $-55°C \leq T_A \leq +125°C$
Power Dissipation ..... 1 Watt
Short Circuit Open Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED DC OPERATING CONDITIONS AND CHARACTERISTICS[1,3,7]

($0°C \leq T_A \leq 70°C$) (V_{CC} = +5V ± 5%, $V_{PP} = V_{CC}$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{OE} = V_{IL}$; $\overline{CE} = V_{IH}$)		10	25	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{OE} = \overline{CE} = V_{IL}$)		57	100	mA	2
I_{PP1}	V_{PP} Current (V_{PP} = 5.25V)			6	mA	2
V_{OH}	Output High Voltage (I_{OH} = -400μA)	2.4			V	
V_{OL}	Output Low Voltage (I_{OL} = 2.1mA)			.45	V	
I_{IL}	Input Leakage Current (V_{IN} = 5.25V)			10	μA	
I_{OL}	Output Leakage Current (V_{OUT} = 5.25V)			10	μA	

AC CHARACTERISTICS[1,2,4]

($0°C \leq T_A \leq 70°C$) (V_{CC} = +5V ± 5%, $V_{PP} = V_{CC}$)

		-5		-6		-7		-8			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to Output Delay ($\overline{CE} = \overline{OE} = V_{IL}$)		300		350		390		450	ns	
t_{CE}	CE to Output Delay ($\overline{OE} = V_{IL}$)		300		350		390		450	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE} = V_{IL}$)		120		120		120		120	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE} = V_{IL}$)	0	100	0	100	0	100	0	100	ns	8
t_{OH}	Address to Output Hold ($\overline{CE} = \overline{OE} = V_{IL}$)	0		0		0		0		ns	

CAPACITANCE

(T_A = 25°C)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	6
C_{OUT}	Output Capacitance	8	12	pF	6

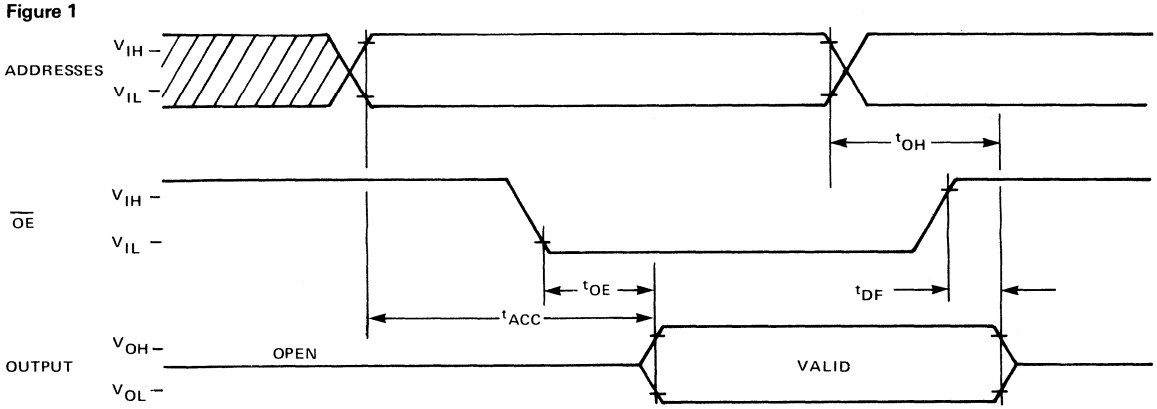
NOTES:

1. V_{CC} must be applied on or before V_{PP} and removed after or at the same times as V_{PP}.
2. V_{PP} and V_{CC} may be connected together (except during programming,) in which case the supply current is the sum of I_{CC} and I_{PP1}. Data Outputs open.
3. All voltages with respect to V_{SS}.
4. Load conditions = ITTL load and 100pF., tr = tf = 20ns, reference levels are 1V or 2V for inputs and .8V and 2V for outputs.
5. t_{OE} is referenced to $\overline{CE}$ or the addresses, whichever occurs last.
6. Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$
7. Typical numbers are for T_A = 25°C and V_{CC} = 5.0V
8. t_{DF} is applicable to both $\overline{CE}$ and $\overline{OE}$, whichever occurs first.
9. $\overline{OE}$ may follow up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without effecting t_{ACC}.

TIMING DIAGRAMS

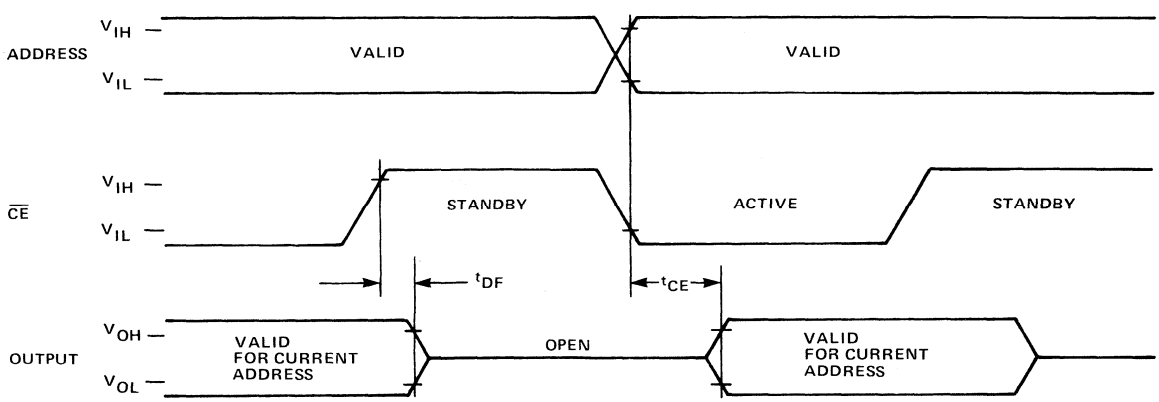
READ CYCLE ($\overline{CE}$ = V_{IL})

Figure 1



STANDBY POWER DOWN MODE ($\overline{OE}$ = V_{IL})

Figure 2



PROGRAM OPERATION[8]

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[1,2]

(T_A = 25°C ± 5°C) (V_{CC} = 5V ± 5%, V_{PP} = 25V ± 1V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current		10	μA	3
V_{IL}	Input Low Level	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}+1	V	
I_{CC}	V_{CC} Power Supply Current		100	mA	
I_{PP1}	V_{PP} Supply Current		6	mA	4
I_{PP2}	V_{PP} Supply Current during Programming Pulse		30	mA	5

AC CHARACTERISTICS AND OPERATING CONDITIONS[1,2,6,7]

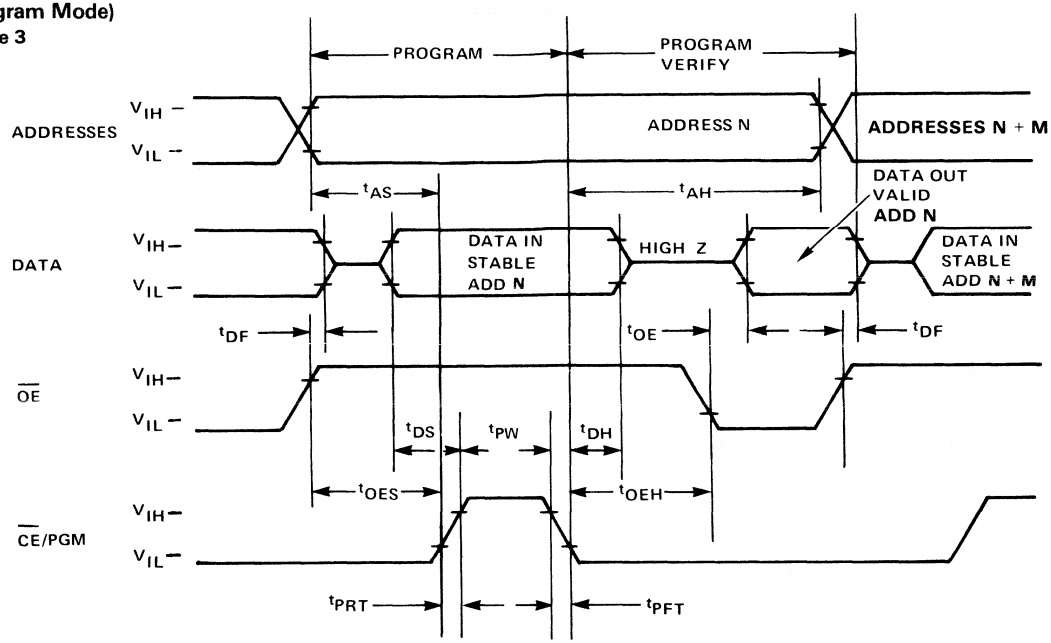
(T_A = 25°C ± 5°C) (V_{CC} = 5V ± 5%), V_{PP} = 25V ± 1V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float	0		120	ns	4
t_{OE}	Output Enable to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:

1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with V_{PP} at 25V.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to +25V.
3. $0.45V \leq V_{IN} \leq 5.25V$
4. $\overline{CE}/PGM = V_{IL}$
5. $\overline{CE}/PGM = V_{IH}$
6. t_T = 20nsec
7. 1V or 2V for inputs and .8V or 2V for outputs are used as timing reference levels.
8. Although speed selections are made for READ operation all programming specifications are the same for all dash numbers.

TIMING DIAGRAM
(Program Mode)
Figure 3



DESCRIPTION CONTINUED

hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525mW maximum active power to 132mW maximum for an overall savings of 75%.

Programming can be done with a single TTL level pulse, and may be done on any individual location either sequencially or at random. The three-state output controlled by the $\overline{OE}$ input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with Mostek's new 5 volt only microprocessors such as the MK3880 (Z80). The MK2716 is packaged in the industry standard 24-pin dual-in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MK2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data/program is fixed and the intention is to produce large numbers of systems, Mostek also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to Mostek, from which the ROM with the desired pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card deck, etc.

READ OPERATION

The MK2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes including READ and STANDBY. A READ operation is accomplished by maintaining pin 18 ($\overline{CE}$) at V_{IL} and pin 21 (V_{PP}) at +5 volts. If $\overline{OE}$ (pin 20) is held active low after addressing (A_0 - A_{10}) have stabilized then valid output data will appear on the output pins at access time t_{ACC} (address access). In this mode, access time may be referenced to $\overline{OE}$ (t_{OE}) depending on when $\overline{OE}$ occurs (see timing diagrams).

POWER DOWN operation is accomplished by taking pin 18($\overline{CE}$) to a TTL high level (V_{IH}). The power is reduced by 75% from 525mW maximum to 132mW. In power down V_{PP} must be at +5 volts and the outputs will be open-circuit regardless of the condition of $\overline{OE}$. Access time from a high to low transition of $\overline{CE}$ (t_{CE}) is the same as from addresses (t_{ACC}). (See STANDBY Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from Mostek will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining V_{PP} at +25V, and $\overline{OE}$ at V_{IH}. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the V_{CC} supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the $\overline{CE}$/PGM pin once addresses and data are stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manor. The program pulse has a minimum width of 45msec and a maximum of 55msec, and must not be programmed with a high level D.C. signal applied to the $\overline{CE}$/PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain $\overline{OE}$ at V_{IH}, V_{PP} at +25, allow addresses and data to stabilize and pulse the $\overline{CE}$/PGM pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with $\overline{CE}$/PGM at V_{IL} will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce V_{PP} from +25V to +5V. V_{PP} should only be used in the PROGRAM/PROGRAM INHIBIT and PROGRAM VERIFY Modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing a ultra-violet lamp with a 12000μW/cm^2 power rating. The lamp should be used without short wave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

PRODUCT PREVIEW

MOSTEK®

8192 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2764(T)-8

FEATURES

- ☐ MK2764 - Organized 8K x 8 bit EPROM
- ☐ Single +5 volt power supply during READ operation
- ☐ Single programming requirement: single location programming with one 50ms pulse
- ☐ Fast access time in READ mode

P/N	ACCESS TIME
MK2764-8	450ns

- ☐ Output Enable ($\overline{OE}$) function for greater system flexibility
- ☐ Power Down mode: 132mW max standby
- ☐ Low power dissipation: 525mW active max
- ☐ Pin compatible with Mostek's BYTEWYDE™ Memory Family
- ☐ Pin compatible mask programmable ROM available: MK37000
- ☐ TTL compatible in all operating modes (except V_{PP} in Program Mode and Program Inhibit)
- ☐ Standard 28 pin DIP with transparent lid
- ☐ Five basic modes of operation (see Table)

DESCRIPTION

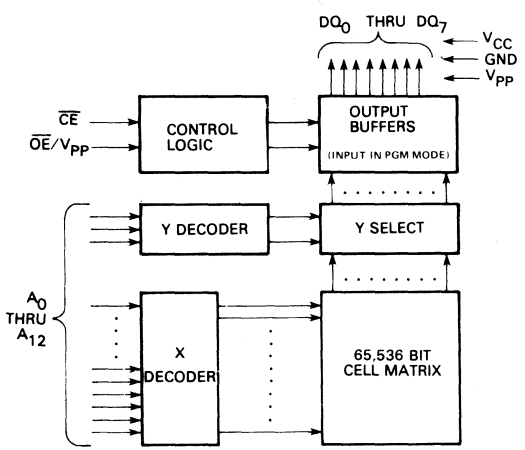
The MK2764 is an 8192 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2764 offers significant advances over hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2764 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525mW maximum active power to 132mW maximum for an overall savings of 75%.

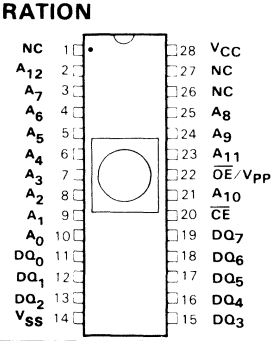
MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}/V_{PP}$	OUTPUTS
PIN	(20)	(22)	
READ	V_{IL}	V_{IL}	Valid
STANDBY	V_{IH}	Don't Care	Open
PROGRAM	Pulsed V_{IH} to V_{IL}	+25	Inputs
DESELECT	V_{IL}	V_{IH}	Open
PROGRAM INHIBIT	V_{IH}	+25	Open
V_{CC} (28) = 5V all modes			

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A_0-A_{12}	ADDRESSES	DQ_0 - DQ_7	DATA OUTPUTS*
$\overline{CE}$	CHIP ENABLE	NC -	NO CONNECTION
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/ PROGRAM	V_{SS} -	GROUND

*Inputs in program mode

MK2764 ERASING PROCEDURE

The MK2764 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. Note that all bits of the MK2764 will be erased. The erasure time is approximately 15 to 20 minutes utilizing an ultraviolet lamp with a 12000μW/cm^2 power rating. The lamp should be used without short wave filters, and the MK2764 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2764. However, it is not recommended that the MK2764 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

MOSTEK®

16K-BIT READ ONLY MEMORY

MK34000(P/J/N)-3

FEATURES

- ☐ 2K x 8 organization with static interface
- ☐ 350ns max access time
- ☐ Single +5V ±10% power supply
- ☐ 330mW max power dissipation
- ☐ Contact programmed for fast turn-around
- ☐ Three programmable chip selects
- ☐ Inputs and three-state outputs — TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF
- ☐ RAM/EPROM pin compatible
- ☐ Pin compatible with Mostek's BYTEWYDE™ Memory Family

DESCRIPTION

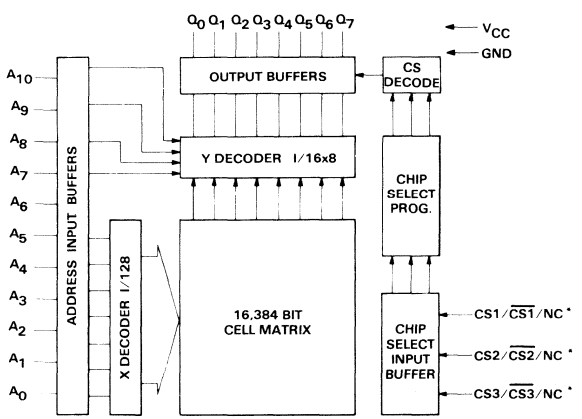
The MK34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK34000 requires a single +5 volt (±10% tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by Mostek's Ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK34000 coupled with the programmable chip select inputs and three-state TTL compatible outputs results in extremely simple interface requirements.

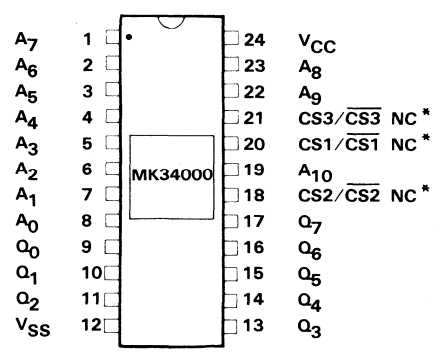
An outstanding feature of the MK34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



*Programmable Chip Selects

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature - Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature - Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-0.5		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C) [6]

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	V	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = -220 μA	2.4	V_{CC}	V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C) [6]

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

CAPACITANCE

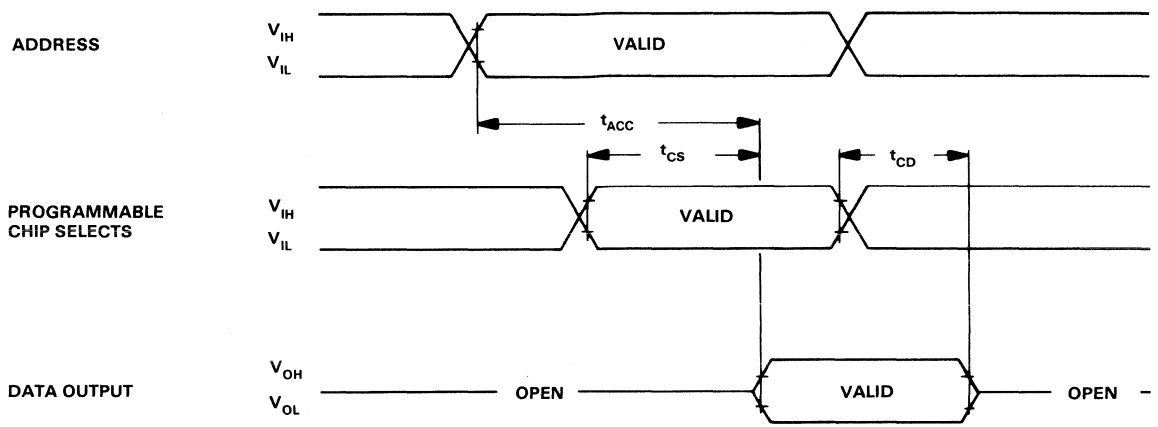
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V (V_{CC} = 5V)
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{I\Delta t}{\Delta V}$ with current equal to a constant 20mA.
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM

Figure 1



*The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	Mostek Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek; may be left blank.
3. Mostek punched card coding format should be used. Punch "Mostek" starting in column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED -i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK

64K-BIT MOS READ-ONLY MEMORY

MK37000 (P/J/N)-4/5

FEATURES

- Organization: 8K x 8 Bit ROM - JEDEC Pinout
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time/Cycle Time

P/N	ACCESS	CYCLE
MK37000-5	300ns	450ns
MK37000-4	250ns	375ns

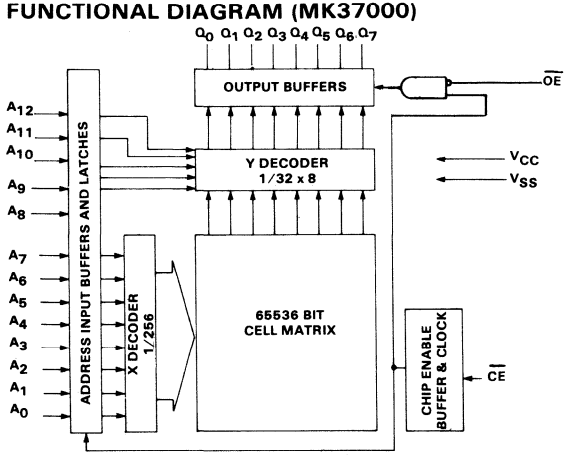
- Mask ROM replacement for MK2764 EPROM
- No Connections allow easy upgrade to future generation higher density ROMs
- Low power dissipation: 220mW max active, 45mW max standby
- $\overline{CE}$ and $\overline{OE}$ functions facilitate Bus control

DESCRIPTION

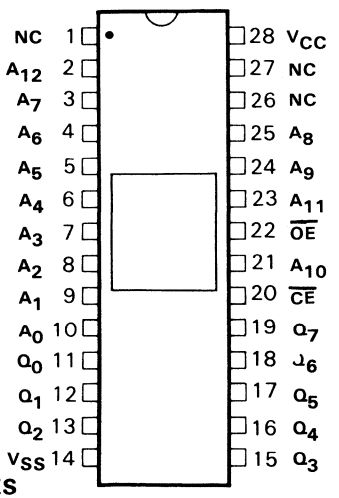
The MK37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to the MK2764 8K x 8 bit EPROM. As a member of the Mostek BYTEWYDE Memory Family, the MK37000 brings to the memory market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MK37000 the lowest power 64K ROM available. Active power is a mere 220mW while standby ($\overline{CE}$ high) is only 45mW. To provide greater system flexibility an output enable ($\overline{OE}$) function has been added using one of the extra pins available on the

FUNCTIONAL DIAGRAM (MK37000)



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

X = Don't Care

PIN NAMES

A0 - A12 - Address	NC - No Connection
$\overline{CE}$ - Chip Enable	$\overline{OE}$ - Output Enable
Q_0 - Q_7 - Outputs	V_{CC} - +5V supply
	V_{SS} - Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS [6]

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS[6]

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)

		-4		-5			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10,000	300	10,000	ns	4
t_{CEA}	$\overline{CE}$ Access Time		250		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		60		75	ns	
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_P	$\overline{CE}$ Precharge Time	125		150		ns	
t_{OEA}	Output Enable Access Time		80		100	ns	
t_{OEZ}	Output Enable Data Off Time		60		75	ns	

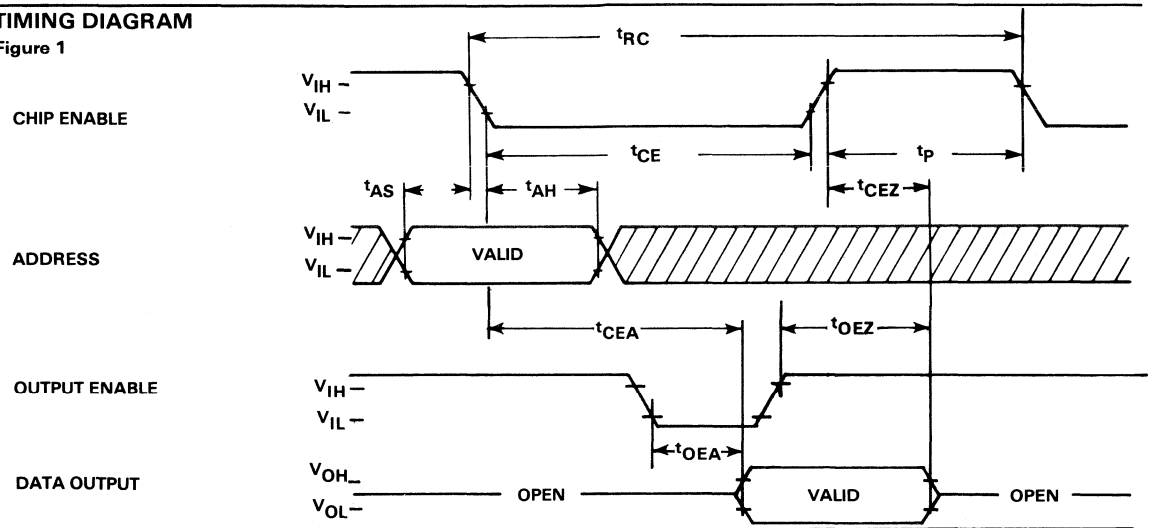
CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM

Figure 1



NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high

DESCRIPTION (Continued)

28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked $\overline{CE}$ mode of operation provides an automatic power down mode of operation. The MK37000 features on chip address latches controlled by the $\overline{CE}$ input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by $\overline{CE}$. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MK37000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MK37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK37000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access

time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time t_P to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A total of (4) 2K x 8 devices would be required to totally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

Acceptable EPROMs for Code Data

Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1

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